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STARGRASP
UH IfA
Internal Only

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Leach IR controller assessment

ARC website http://www.astro-cam.com/

Positive aspects

Wide user base and MIRSI experience

- Multiple organizations have successfully fielded facility grade H2RG, Leach Gen III(?) instruments.
  - A good source of real on telescope information is the CFHT WIRCAM. Be aware that they were pushing for faster readout, high background guiding too.
- Charles: should write a paragraph describing his MIRSI experience. Please comment on the experienced reliability, amount of down time and fixes.

Pre-existing software for the H2RG

- Charles: to summarize what ARC provides, specifically what clocking modes are supported. this can be added to Reference Section below.
- Hubert informed me that Don's system used Ev's code which was a major rewrite of the Leach code at the time.

MKIR software development

- Steps should be taken to insure that the MKIR and IRTF developments are clearly defined and known to scope what is shared and independent.

MIRSI hardware and common spares?

- Charles and Eric: are there common upgrades or spares? What about the PC hardware and software?

Hubert's analysis code

- Hubert's analysis code should be very portable to the Leach generated data since that's he started with to generate the SGIR code.

Negative aspects

ARC gen III "hangs" and software driver

- There is widespread experience with "hangs" on with Gen III fiber interface. Hubert's experience with the Hilo system was that a configuration (clocking, readout speed, etc) could be found that allowed reliable readouts but changes to that configuration could result in hangs. I'd estimate that this is a medium level risk to getting particular modes reliably working (but not an overall risk to the projects).

Computer interface hardware dependency

- Assuming an ARC64: 250 MHz PCI INTERFACE BOARD, GEN III, the PCI fiber interface will face a very limited lifetime on the PC side. I would predict that the PCI interface will be progressively phased out in a 3-5 year time span. This is more than a hardware issue since operating system changes may drop or change support for the interface. At the very least, the IRTF should plan on purchasing full PC platform spare(s) with completely copied (frozen) operating system software. Alternatively, the IRTF could plan and budget for an upgrade (presumably from ARC) in the same time frame.

Physical Size

- The ARC controller is ~X4 times larger than SGIR. For NSFCAM I doubt if this is a problem. For Spex and ISHELL it may be. There are two type of housings and I don't offhand know if the Spex and ISHELL would two large,two small or a combiination.
  - Large housing: 12-slot unit essentially consists of two 6-slot controller housing bolted together, but with a 12-slot backplane. Controller housing dimensions 13.25 x 6.75 x 10.5 inches 33.30 x 16.2 26.67 cm Controller weightb21 lbs. = 9.5 kg.
  - Small housing: The 6-slot closed controller housing contains the controller backplane, an ARC73 power control board, and a machined aluminum enclosure for mounting up to six controller boards. An internal blower circulates the bulk of the air inside the enclosure, while allowing a some air to be drawn from outside. Alternatively, the housing can be sealed and outfitted with a liquid heat exchanger. The controller housing has removable front and side panels to allow easy access for servicing. Internal shutter wiring and fiber optic cables are included. Controller housing dimensions 13.25 x 6.75 x 5.5 inches 33.30 x 16.20 x 14.0 cm Controller weight 14 lbs. = 6.4 kg.
- Eric?: determine what is needed.

Power supply noise

- There are documented reports and IfA experience with the ARC power supplies. The IRTF should adapt the HP66000 supplies for ARC use. This is a low risk task.

Dynamic Range and ARC46 gain

- Eric: should calculate the full well dynamic range of the ARC video chain in both settings. I've included an excerpt of the manual in the Reference Section below.

Longevity of the Freescale DSP and other components

- The DSPs that run the ARC system used to be Motorola now Freescale components and are relatively old devices.
- Eric: should do an industry check and form an opinion on how long they well be continued. He should do this for the RAM also.

Issues to resolve

Should the IRTF modify or design their own bias filters for the critical biases?

ANU chose to do this, I've attached a reference here: https://irtf.stargrasp.org/attachment/wiki/SG-IRDetectorsWorkpage/LBNL-61039.pdf?format=raw

> For Fowler-32 sampling in 300s exposures, the scatter in the global mean is 5.8e- for the ARC (Leach) biases, reducing to 1.1e- after per-channel top-bottom reference pixel subtraction. The ANU bias board is much more stable delivering less scatter (0.7ADU rms) in the uncorrected global mean. This reduces to just 0.2e- 7 rms after reference pixel subtraction. Although the reference pixel subtraction attenuates the zero point drift by a factor of 4 or 5, it is clearly beneficial to have stable biases in the first place. Further work is planned to measure the attenuation more directly.

Spares policy

The IRTF should come up with a spares policy for not only the custom ARC hardware, but also the PC platform, operating system and operational software.

Reference and window outputs

Eric: should find out what is normally supported in hardware.
Charles: should find out what is supported in software.

Reference Information

Electronics

gain and dynamic range

- Leach ARC46 users manual: https://irtf.stargrasp.org/attachment/wiki/SG-IRDetectorsWorkpage/ARC46_UsersManual.pdf?format=raw

  The outputs of each buffer stage are brought to an op amp configured as a differential amplifier with unity gain. After this differential stage the video signal is fed into the inverting input of an AD829 op amp configured with a gain of x5. A DC offset nulling level is fed into the non-inverting input of this gain stage, providing for nulling of the IR array over a range of -3 to +5 volts. Following this is an integrator stage whose gain is proportional to the integration time and inversely proportional to the product of its input resistance and feedback capacitance. The feedback

capacitance is fixed at 1nF, while the input resistance has two software selectable values, 4k for low gain, slow readouts or 1k for high gain, fast readout. Note that the shortest pixel time is 2.6us/pix for a 32 channel detector, which is limited by the fiber optic speed of 12.5 Mpixels/sec.

The A/D converters are configured with an input voltage range of -2.5 to +2.5 volts, so this is about a factor of 10 overall analog gain. The input amplifier stage provides a gain of 5, while the integration time of nearly 2 microsec with the integrator RC values of 1k and 1nf provide an integrator gain of close to 2, for an overall gain of about x10.

ADC and bias circuit

- Eric: please get the ARC schematics from MKIR. We will want to document which ADC it uses, the gain, input range, uv/adu and full well in adus.

Software