NASA IRTF / UNIVERSITY OF HAWAII

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ISHELL ARRAY CONTROLLER OVERVIEW

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Revision History

Revision No.	Author & Date	Approval & Date	Description

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1 Introduction / Document Purpose

The NASA IRTF is upgrading NSFCAM and Spex, while also building a new instrument iSHELL. NSFCAM, Spex, and iSHELL use a H2RG. Spex and iSHELL also has an Aladdin 51x512 array for imaging/guiding. In 2012-01, the IRTF select the Astronomic Research Cameras (ARC) controller to be the array controller for these instruments. The effort to customize the ARC controllers for the IRTF is called IARC. This document will presents an overview of controller design for SpeX and iSHELL.

2 Requirements

A summary of the array controller requirement is presented in this section.

The following documents provide some background information on the iSHELL, SpeX, and NSFCAM controller requirements.

Array Controller Requirements. The overall science requirements for iSHELL, SpeX, and NSFCAM were described in 2009.
http://irtfweb.ifa.hawaii.edu/~s2/hist/0907_array_controller_requirements/CONTROLLER_SRD_24June09.pdf

Evaluation of the ARC Controller for the NASA IRTF. A discussion the ARC controller system and it's adaption by the IRTF was held in Feb 2012.
http://irtfweb.ifa.hawaii.edu/~iarc/1201_ARC_Eval/Evaluation_of_the_ARC_Controller_for_the_NASA-Document.pdf

From these documents, a summary of the requirement is presented

2.1 Summary of H2RG Requirements

- Supports 2048x2048 array readouts with 32 channels
- System Throughput - Be able to support full frame rate of 300K pixel per seconds (fastest desired frame rate for the H2RG). The controller should be able to support continuous coaddition/subtraction of back-to-back readout of the full array at 300K pixels/second or 0.436 seconds/image. The maximum number of continuous frame supported is 64000.
- Adjustable Frame Rates with the following values: 300kHz, 200kHz, 100Hz or pixel/sec. (0.43, 0.86, 1.31 seconds per full Frame Readout)
- Well Depth > 50,000e.

2.2 Examples of H2RG Requirements

Program	Requirements
Faint Object Spectroscopy, Slow readout, multiple NDR. ie: itime > 60s (600 typical), coadd=1, FR=1.3, NDR=24	5e RMS, 2e RMS goal
Bright Object Spectroscopy, Fast readout, ie: itime 0.5-10 (1 typical), coadd=10, FR=0.43, ndr=1	100e RMS, 30e RMS goal
Standard Star Spectroscopy itime 10-60, coadds=6, FR=0.43/1.3, ndr=24	15e RMS, 5e RMS goal

Movie Mode itime=0.1-0.5, coadd=1, FR=0.44, NDR=1, Subarray=1024x600, continuous 1 hour.	30e RMS, 10e RMS goal

2.3 Summary of Aladdin Requirements

- Supports 512x512 array readouts with 8 channels.
- System Throughput - Be able to support full frame rate of 270K pixel per seconds (fastest desired frame rate for the Aladdin). The controller should be able to support continuous coaddition/subtraction of back-to-backup readout of the full array at 270K pixels/second, or 0.1 seconds/image. The maximum number of continuous frame supported is 64000.

2.4 Examples of Aladdin Requirements

Program	Requirements
Imaging, Faint ei: itime=5.0, Coadd=1, FR=0.24, NDR=12	30e RMS, 10e RMS goal
Bright Object Spectroscopy, Fast readout, ie: itime 0.5-10 (1 typical), coadd=10, FR=0.1, ndr=1	100e RMS, 30e RMS goal

2.5 General Software parameter, modes of operations, and requirements

This section provides list the general input parameter, modes of operation, and other software features that the IARC software will support.

time - The integration time, or time between Pedestal&Sample readouts.. Integration time input range is 0.0001 to 1800.000 seconds, millisecond resolution. Actual minimum time is the time to clock out the Array (Frame Rate).

Coadd - Coadds of integrations. Range is 1 to 1000.

cbmode - Clock buffer mode controls reset-sample scheme used to produce an image. Three mode are desired.

- fs - Fowler Single. 1 coadd is [Reset][Sample x ndr]. Integration time is the exposure time of the samples
- fd - Fowler Double. 1 codadd is [Reset][Pedestal x ndr][Sample x ndr]. Integration time is Sample-Pedestal.
- ramp - sample of the ramp. 1 coadd is [Reset][sample1] ..[sample N]. Individual images are used to define a slope of each pixel. The final image is a fit based on the N samples.

ndr – Number of successive non-destructive reads done during fs/fd cbmode to obtain a sample or pedestal images. Range is 1 to 128 (but 32 is the typical default value). The number of NDRs is reduced to achieve the requested itime exposure

rsample - Number of Ramp Sample. Indicates how much readouts are used for CBmode ramp. Range is 3 to 10.

Frame Rate - The Frame Rate controls the speed used to clock out the device. The software should allow adjustments to the frame rate. Longer integration could use slower rates to improve noise performance. The exact implementation is array dependent.

Subarrays - Support up to 3 subarrays. Allow the user to define upto 3 sub-array indicated the desire pixels to sample.

- Subarray array are specified by: x y wid hgt.
- Subarray can overlap, it the job of the controller to read out the pixel specified by the sub array parameters.

Background Resets - While the camera is idle, background reset of the array are performed. These reset can be global resets, or pixel level resets. If pixel level resets, the frame rate should match the observing readout frame rates.

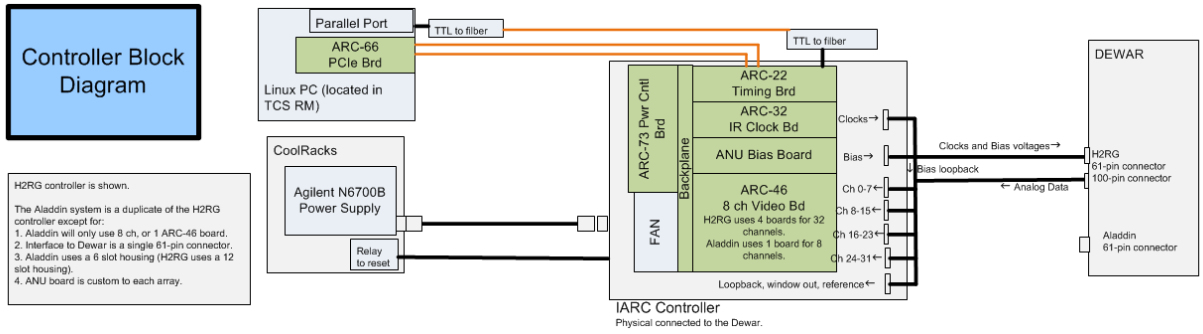
Gracefult Aborts - The ability to abort an operation with minimal overhead., ie: "opps, I did a GO with 1000 coadd and 300 seconds, how can I stop it".

Image timestamps. The time when the readouts begin needs to be time stamped with an accuracy of 1 millisecond.

3 IARC Design

This section describes the IARC design for both the H2RG and Aladdin systems.

3.1 Controller Block Diagram



This controller block diagram illustrates key concept on the IARC design.
Linux PC

- Runs the CentOS 6.x Linux OS.
- Instrument software is our in-house custom built IRTF Instrumentation Software . This software uses the ARC API and PCIe device drivers.
- The ARC-66 PCIe board is installed in this PC.
- A parallel port interrupt is used to timestamp the shutter output form the ARC-22 board for image timestamps.

Cool Rack Electronic

- Agilent N6700B have replace the stock ARC power supplies for IRTF instruments.

IARC Controller

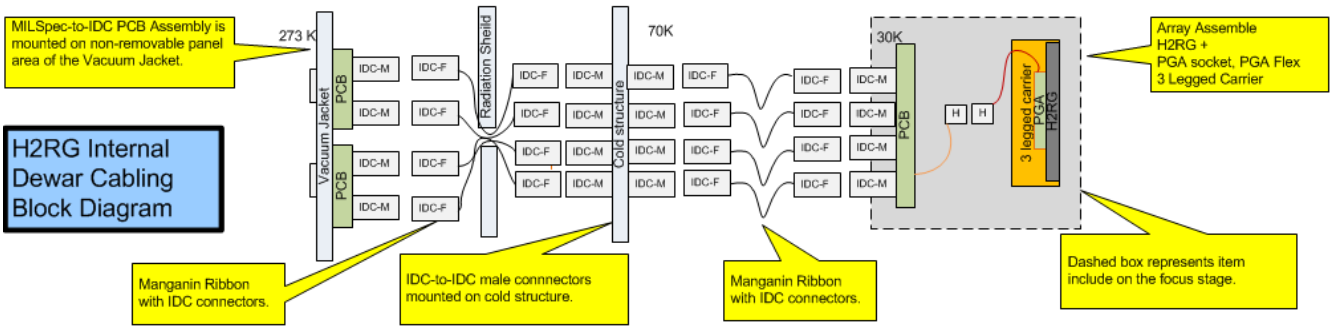
- ARC controller with ARC-73 Power Control Board, ARC-22 Timing Board, ARC-32 IR Clock Board. The H2RG system will have 4 ARC-46 Video Boards (32 channels). The Aladdin system will have 1 Video Board (8 channels).
- An in-house build 'ANU Bias Board' is used to provide critical non-clocking voltages to the array, replacing DAC channels normally provided by the ARC-46 Video Boards.
- The H2RG uses a 12-Controller Housing (ARC-72) as it hosts 7 boards. The Aladdin uses a 6 slot Controller Housing (ARC-70) to host 4 boards.

Interface Cable to Dewar

- A custom cable is built to connect the ARC boards to the MilSpec connection on the IRTF Dewars.
- Based on the current NSFCAM design. However, for Spex/iSHELL reorganized the pin assignments in the cabling to separate the clock and data channels. The Dewar's connector interface will change from 2 61-pin connector to a 61-pin and 100-pin connector.
- The interface cable plug directly into the 50-pin DB connector in the ARC controller boards. An extra connector exists to provide addition analog channels to the system. This extra connector contains ANU bias voltages, signal grounds, and the H2RG's Window out and reference pixels.

3.2 H2RG Internal Dewar Cabling

The following diagram illustrates the internal cabling for the H2RG.

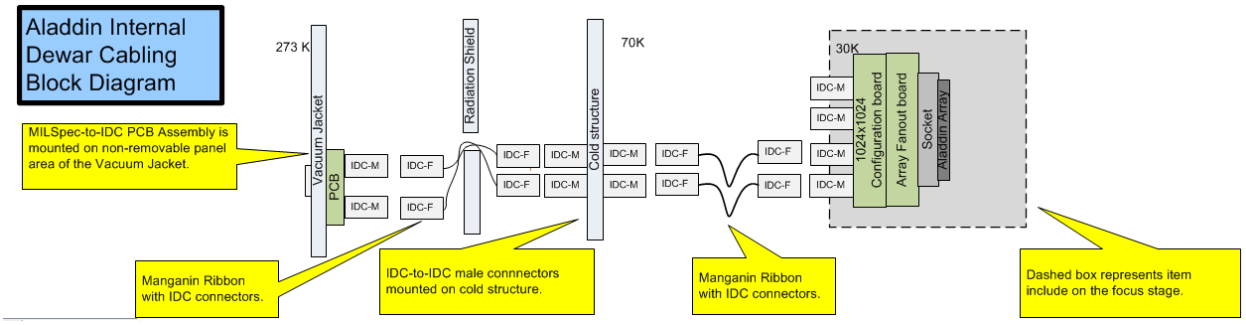


Design is based the on current NSFCAM H2RG system. The NSFCAM H2RG hardware was design and build in 2012. NSFCAM was upgraded to the IARC controller in 4Qtr 2012, and is being re-commissioned at the IRTF during the 1Qtr 2013.

For iSHELL, the Cryo Config Board and Connector-PBC will be remanufactured to order to separate the clocking and analog data channels, and change one 61-pin connector to a 100-pin connector. A design change in the array mount also requires a new layout for the Cryo Config Board.

3.3 Aladdin Internal Dewar Cabling

The following diagram illustrates the internal cabling for the Aladdin Array



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The internal cabling for the Aladdin array will be based on the current SpeX design. SpeX itself will be have it current controller replaced with the IARC controller in 1st Qtr 2014. SpeX's internal cabling will not be changed. For iSHELL we will reproduce the SpeX hardware.

4 IARC Performance and Testing

CL to do. Provide data on how well nsfcam's hardware is doing relative to the requirements listed above.