

OPERATIONS MANUAL

PCM-I/O48

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1.0 GENERAL INFORMATION

1.1 FEATURES

- * 48 I/O lines configured as six, 8-bit parallel I/O ports
- * Designed to interface directly to 2 standard industrial isolation I/O module racks (Opto-22)
- * Dual 50-pin header connectors
- * Single 8-bit PC/104 module compatible
- * Uses two 82C55A (NEC 71055) PPIs
- * No power glitching on I/O lines
- * Single +5 volt operation
- * Extended operational temperature range: -40° to +85° Centigrade

GENERAL INFORMATION

1.2.1. **PCM-I/O48** - The PCM-I/O48 is a compact, PC/104 multimodule, general purpose 48-line parallel I/O controller based upon two 82C55A Programmable Peripheral Interface (PPI) devices. These lines are organized as 2 groups of three 8-bit I/O ports that interface directly to 2 independent industry standard 4, 8, 16, and 24-I/O module mounting racks (Opto-22, Gordos, etc.).

1.2.2. **PC/104 Interface** - The PCM-I/O48 is I/O port mapped with each channel having a unique port address determined by the base board. The board will work with either a regular NMOS/TTL or CMOS CPU base board.

1.2.3. **Parallel Controller** - Two 82C55A Programmable Peripheral Interface (PPI) devices are on the PCM-I/O48 board. Each chip is independent from the other and each supports 24 I/O pins which may be individually programmed in 2 groups of 12 in 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In Mode 1 each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group for handshaking. Although an 82C55A offers great flexibility as a general purpose parallel interface device, it would be programmed in Mode 0 for use with standard I/O mounting racks. This means that the digital signal conditioning modules must be grouped in sets of 8 as either input or output. The signal levels are TTL compatible. Each I/O line has a 10K ohm pull-up resistor to keep the input from floating.

1.2.4. **I/O Connector** - Each 82C55A has its 24 I/O lines connected to a separate 50-pin male right angle connector. The 24 data lines are alternated with 24 ground lines for reduced noise and crosstalk. The pinout is compatible to an industry standard 4 to 24 position I/O module mounting rack (Opto-22, Crydom, Gordos, etc.) for use with high level AC and DC signal interfacing. A 50 conductor ribbon cable such as the WinSystems CBL-115-4 connects the PCM-I/O48 to one I/O rack. Two cables are required to fully utilize this card, one for each rack. The cable will interface directly to a 4, 8, 16 or 24 module rack.

J1 and J2 - Rack I/O Connector

Pin	Description	Pin	Description
1	PA0	2	Gnd
3	PA1	4	Gnd
5	PA2	6	Gnd
7	PA3	8	Gnd
9	PA4	10	Gnd
11	PA5	12	Gnd
13	PA6	14	Gnd
15	PA7	16	Gnd
17	PB0	18	Gnd
19	PB1	20	Gnd
21	PB2	22	Gnd
23	PB3	24	Gnd
25	PB4	26	Gnd
27	PB5	28	Gnd
29	PB6	30	Gnd
31	PB7	32	Gnd
33	PC0	34	Gnd
35	PC1	36	Gnd
37	PC2	38	Gnd
39	PC3	40	Gnd
41	PC4	42	Gnd
43	PC5	44	Gnd
45	PC6	46	Gnd
47	PC7	48	Gnd
49	+5v	50	Gnd

1.3 SPECIFICATIONS

Electrical

PC/104 compatible for 8-bit operation

Parallel Interface: 48 I/O lines, TTL compatible

Power Requirements: +5V \pm 10% at 20mA typ. (No Load)

Mechanical

Dimensions: 2.85 x 3.70 inches

Connectors

PC/104: 18/36-pin 0.100" dual row male

Parallel: Two 50-pin dual 0.100" headers

Mating Connector Panduit 050-050-455 or equivalent

Jumpers: 0.025" square posts

Environmental

Operating Temperature: -40°C to +85°C

Non-condensing relative humidity: 5% to 95%

2.0 USER INFORMATION

2.1. PC/104 MODULES

2.1.1. The PCM-I/O48 is a general purpose parallel I/O board that is designed for use on the PC/104 I/O bus. The PC/104 bus is now a "Defacto Standard" for small add-on boards for use on the STD BUS and other computer board products.

2.2. I/O ADDRESSING

2.2.1. The PCM-I/O48 uses an EPAL for I/O address decoding. The starting address for the board is controlled by jumper block J5. Each decoded I/O address block takes eight I/O addresses. The address decoder is programmed for 16 different starting addresses that range from 0100H to 0178H on eight byte boundaries. See Table 2-1 below.

NOTE: The I/O ports associated with connector J1, begin at the **BASE_ADDRESS + 4**, the I/O ports for J2 begin at **BASE_ADDRESS + 0**.

TABLE 2-1
J5 JUMPER BLOCK I/O ADDRESSING
STARTING BASE ADDRESSES

100H	108H	110H	118H	120H	128H
1o--o2	1o o2	1o--o2	1o o2	1o--o2	1o o2
3o--o4	3o--o4	3o o4	3o o4	3o--o4	3o--o4
5o--o6	5o--o6	5o--o6	5o--o6	5o o6	5o o6
7o--o8	7o--o8	7o--o8	7o--o8	7o--o8	7o--o8
9o o10	9o o10	9o o10	9o o10	9o o10	9o o10
130H	138H	140H	148H	150H	158H
1o--o2	1o o2	1o--o2	1o o2	1o--o2	1o o2
3o o4	3o o4	3o--o4	3o--o4	3o o4	3o o4
5o o6	5o o6	5o--o6	5o--o6	5o--o6	5o--o6
7o--o8	7o--o8	7o o8	7o o8	7o o8	7o o8
9o o10	9o o10	9o o10	9o o10	9o o10	9o o10
160H	168H	170H	178H		
1o--o2	1o o2	1o--o2	1o o2		
3o--o4	3o--o4	3o o4	3o o4		
5o o6	5o o6	5o o6	5o o6		
7o o8	7o o8	7o o8	7o o8		
9o o10	9o o10	9o o10	9o o10		

NOTE: J5 9-10 MUST BE LEFT OPEN AND IS FOR BOARD TEST ONLY

J2 I/O address: **BASE_ADDRESS + 0**
J1 I/O address: **BASE_ADDRESS + 4**

2.3. CONNECTOR PIN-OUTS

2.3.1. The PCM-I/O48 consists of two 8255/82C55 (NEC 71055) Programmable Peripheral Interface (PPI) devices. Each PPI device has 24 lines of parallel that can be programmed for three different modes of operation. All of the parallel I/O lines from each PPI have a 10K pull-up resistor and is brought out to one of the two 50 pin connectors on the board. See Figures 2-1 and Figures 2-2 for the connector pin-outs. The mating connector for J1 or J2 is a Panduit 050-050-455 or equivalent.

NOTE:

For applications that require boards to be stacked on top of the PCM-I/O48, it will not be possible to use a strain relief on connector J2.

2.4. PROGRAMMING

2.4.1. Programming the PCM-I/O48 consists of outputting several command words to the PPI device that is to be used. The I/O address of the PCM-I/O48 is controlled by the jumper block J5, see section 2-2. The PCM-I/O48 powers up in MODE 0 with all lines set to inputs. Most PCM-I/O48 applications will use MODE 0 for input and output operations. Port 0 and Port 1 of the 71055 can be only accessed as bytes whereas Port 2 can be accessed as upper and lower 4 bits. See the programming example below for an example of how to initialize the 71055 for Ports 0, 1, and 2. For programming and examples for the 71055 (82C55) the user should consult the appendix for further information.

```
/* Sample 8255 initialization for PCM-I/O48 */

/* Define Addresses of the Data and Command Ports */

#define PORT_BASE 0x100          /* Board addressed at 100 Hex */

#define PIO1_A          PORT_BASE
#define PIO1_B          PORT_BASE + 1
#define PIO1_C          PORT_BASE + 2
#define PIO1_CMD        PORT_BASE + 3

#define PIO2_A          PORT_BASE + 4
#define PIO2_B          PORT_BASE + 5
#define PIO2_C          PORT_BASE + 6
#define PIO2_CMD        PORT_BASE + 7

/* Group 1 direction commands */

#define PORT2_IN_LSB    0x01          /* LSB of port 2 for input */
#define PORT2_OUT_LSB   0x00          /* LSB of port 2 for output */
#define PORT1_IN        0x02          /* Port 1 for input */
#define PORT1_OUT       0x00          /* Port 2 for output */

/* Group 1 mode commands */

#define MODE1N2_0       0x80          /* Mode 0 for group 1 */
#define MODE1N2_1       0x84          /* Mode 1 for group 1 */
```

```
/* Group 0 direction commands */
```

```
#define PORT2_IN_MSB      0x08      /* MSB of port 2 for input */  
#define PORT2_OUT_MSB    0x00      /* MSB of port 2 for output */  
#define PORT0_IN         0x10      /* Port 0 for input */  
#define PORT0_OUT        0x00      /* Port 0 for output */
```

```
/* Group 0 mode commands */
```

```
#define MODEON2_0         0x80      /* Mode 0 for group 0 */  
#define MODEON2_1         0xA0      /* Mode 1 for group 0 */  
#define MODEON2_2         0xC0      /* Mode 2 for group 0 */
```

```

main()
{
  unsigned mode_word;

      /* Example #1 : Init all 48 lines for input */

mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_IN | PORT1_IN | PORT2_IN_MSB |
  PORT2_IN_LSB;
  outp(PIO1_CMD,mode_word); /* Init the first chip */
  outp(PIO2_CMD,mode_word); /* and then the second chip */

  /* Example #2 : Init PIO1 for
      PORT 0 = input
      PORT 1 = output
      PORT 2 LSB = input
      PORT 2 MSB = output

      Init PIO2 for

      PORT 0 = output
      PORT 1 = output
      PORT 2 LSB = output
      PORT 2 MSB = input
  */

mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_IN | PORT1_OUT |
  PORT2_IN_LSB | PORT2_OUT_MSB;
  outp(PIO1_CMD,mode_word); /* Init the first chip as desired */

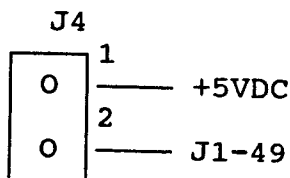
mode_word = MODE0N2_0 | MODE1N2_0 | PORT0_OUT | PORT1_OUT |
  PORT2_OUT_LSB | PORT2_IN_LSB;
  outp(PIO2_CMD,mode_word); /* Init the second chip */
}

```

**FIGURE 2-1
J2 I/O PIN-OUT**

DEVICE #	PPI #	CONNECTOR	PIN #	8255/82C55 FUNCTION
U1	0	J2	1	PA0
			3	PA1
			5	PA2
			7	PA3
			9	PA4
			11	PA5
			13	PA6
			15	PA7
			17	PB0
			19	PB1
			21	PB2
			23	PB3
			25	PB4
			27	PB5
			29	PB6
			31	PB7
			33	PC0
			35	PC1
			37	PC2
			39	PC3
			41	PC4
			43	PC5
			45	PC6
			47	PC7
			49	J4 + 5VDC JUMPER

NOTE: All even numbered pins on J2 are ground.

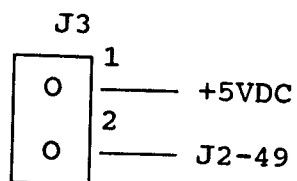


NOTE: Installing a jumper on J4 will connect +5 VDC to J2-49.

**FIGURE 2-2
J1 I/O PIN-OUT**

DEVICE #	PPI #	CONNECTOR	PIN #	8255/82C55 FUNCTION
U4	1	J1	1	PA0
			3	PA1
			5	PA2
			7	PA3
			9	PA4
			11	PA5
			13	PA6
			15	PA7
			17	PB0
			19	PB1
			21	PB2
			23	PB3
			25	PB4
			27	PB5
			29	PB6
			31	PB7
			33	PC0
			35	PC1
			37	PC2
			39	PC3
			41	PC4
			43	PC5
			45	PC6
			47	PC7
			49	J3 + 5VDC JUMPER

NOTE: All even numbered pins on J1 are ground.



NOTE: Installing a jumper on J3 will connect +5 VDC to J1-49.

APPENDIX

Description

The μ PD71055 is a low-power CMOS programmable parallel interface unit for use in microcomputer systems. Typically, the unit's three I/O ports interface peripheral devices to the system bus.

Features

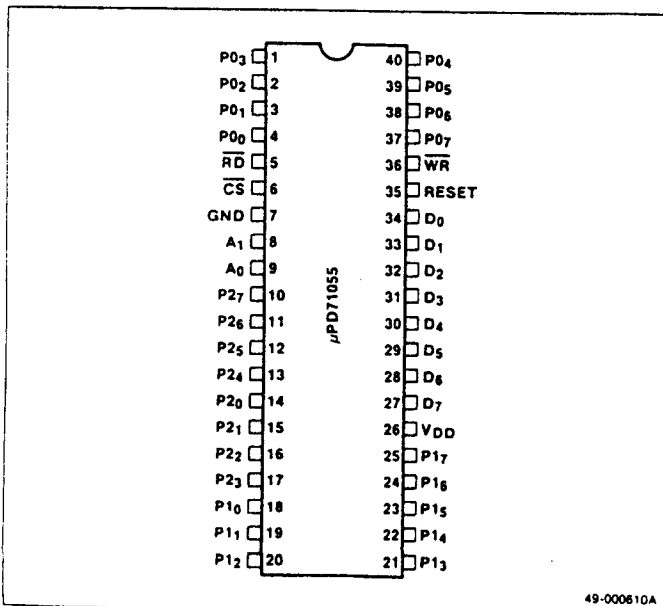
- Three 8-bit I/O ports
- Three programmable operation modes
- Bit manipulation command
- Microcomputer compatible
- CMOS technology
- Single +5 V \pm 10% power supply
- Industrial temperature range: -40 to +85 °C
- 8 MHz and 10 MHz

Ordering Information

Part Number	Clock (MHz)	Package
μ PD71055C-8	8	40-pin plastic DIP
C-10	10	
G-8	8	44-pin plastic QFP (P44G-80-22)
GB-8	8	44-pin plastic QFP (P44GB-80-3B4)
GB-10	10	
L-8	8	44-pin PLCC
L-10	10	

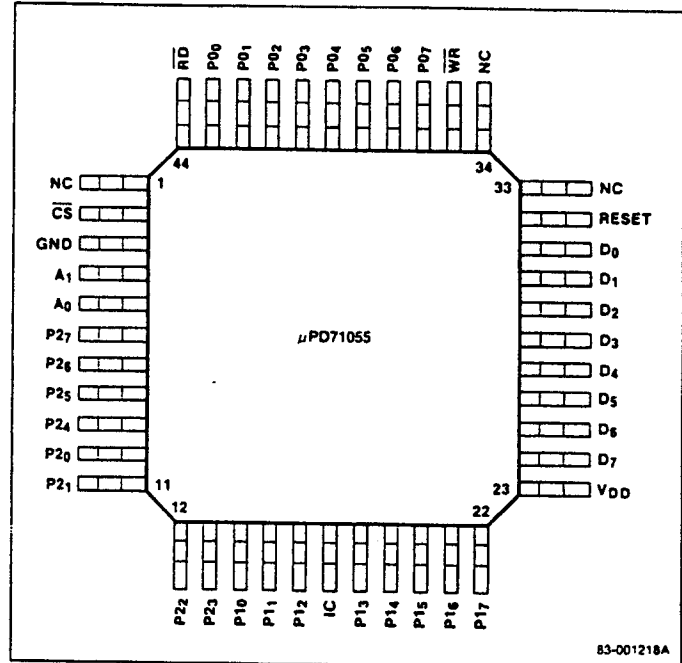
Pin Configurations

40-Pin Plastic DIP



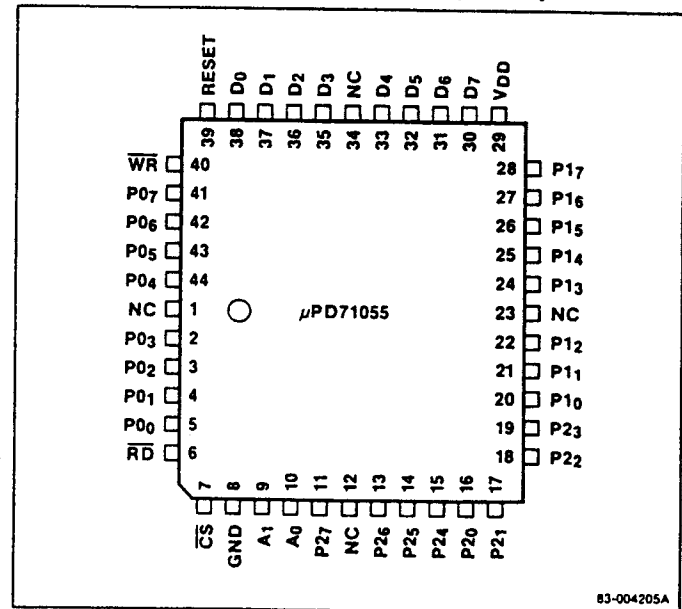
49-000610A

44-Pin Plastic QFP



83-001218A

44-Pin Plastic Leaded Chip Carrier (PLCC)



83-004205A

5e

Pin Identification

Symbol	Function
\overline{CS}	Chip select input
GND	Ground
A ₁ , A ₀	Address inputs 1 and 0
P0 ₇ -P0 ₀	I/O port 0, bits 7-0
P1 ₇ -P1 ₀	I/O port 1, bits 7-0
P2 ₇ -P2 ₀	I/O port 2, bits 7-0
IC	Internally connected
V _{DD}	+5 V
D ₇ -D ₀	I/O data bus
RESET	Reset input
\overline{WR}	Write strobe input
\overline{RD}	Read strobe input
NC	No connection

Pin Functions**D₇-D₀ [Data Bus]**

D₇-D₀ make up an 8-bit, three-state, bidirectional data bus. The bus is connected to the system data bus. It is used to send commands to the μ PD71055 and to send data to and from the μ PD71055.

 \overline{CS} [Chip Select]

The \overline{CS} input is used to select the μ PD71055. When $\overline{CS} = 0$, the μ PD71055 is selected and the states of the D₇-D₀ pins are determined by the \overline{RD} and \overline{WR} inputs. When $\overline{CS} = 1$, the μ PD71055 is not selected and its data bus is high-impedance.

 \overline{RD} [Read Strobe]

The \overline{RD} input is set low when data is being read from the μ PD71055 data bus.

 \overline{WR} [Write Strobe]

The \overline{WR} input should be set low when data is to be written to the μ PD71055 data bus. The contents of the data bus are written to the μ PD71055 at the rising edge (low to high) of the \overline{WR} signal.

A₁, A₀ [Address]

The A₁ and A₀ inputs are used in combination with the \overline{RD} and \overline{WR} signals to select one of the three ports or the command register. A₁ and A₀ are usually connected to the lower two bits of the system address bus (table 1).

 \overline{WR} [Write Strobe]

The \overline{WR} input should be set low when data is to be written to the μ PD71055 data bus. The contents of the data bus are written to the μ PD71055 at the rising edge (low to high) of the \overline{WR} signal.

A₁, A₀ [Address]

The A₁ and A₀ inputs are used in combination with the \overline{RD} and \overline{WR} signals to select one of the three ports or the command register. A₁ and A₀ are usually connected to the lower two bits of the system address bus (table 1).

Table 1. Control Signals and Operation

\overline{CS}	\overline{RD}	\overline{WR}	A ₁	A ₀	Operation	μ PD71055 Operation
0	0	1	0	0	Port 0 to data bus	Input
0	0	1	0	1	Port 1 to data bus	Input
0	0	1	1	0	Port 2 to data bus	Input
0	0	1	1	1	Use prohibited	
0	0	0	x	x		
0	1	0	0	0	Data bus to port 0	Output
0	1	0	0	1	Data bus to port 1	Output
0	1	0	1	0	Data bus to port 2	Output
0	1	0	1	1	Data bus to command register	Output
0	1	1	x	x	Data bus high impedance	
1	x	x	x	x		

RESET [Reset]

When the RESET input is high, the μ PD71055 is reset. The group 0 and the group 1 ports are set to mode 0 (basic I/O port mode). All port bits are cleared to zero and all ports are set for input.

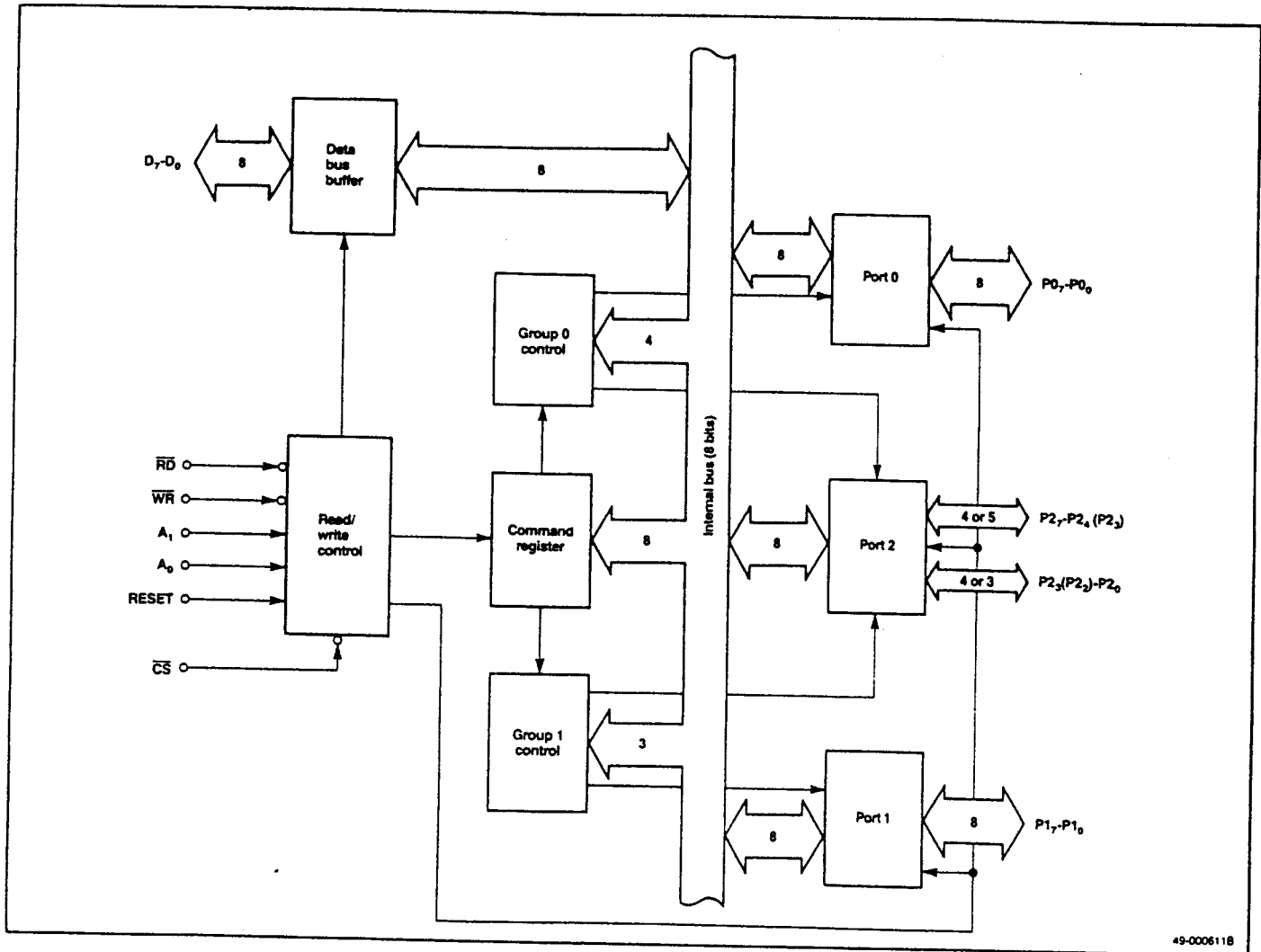
P0₇-P0₀, P1₇-P1₀, P2₇-P2₀ [Ports 0, 1, 2]

Pins P0₇-P0₀, P1₇-P1₀, and P2₇-P2₀ are the port 0, 1, and 2 I/O pins, bits 7-0, respectively.

IC [Internally Connected]

Pins marked IC are used internally and must be left unconnected.

Block Diagram



49-0006118

5e

Functional Description

Ports 0, 1, 2

The μPD71055 has three 8-bit I/O ports, referred to as port 0, port 1, and port 2. These ports are divided into two groups, group 0 and group 1. The groups can be in one of three modes, mode 0, mode 1, and mode 2. Modes can be set independently for each group.

When port 0 is in mode 0, port 0 and the four upper bits of port 2 belong to group 0, and port 1 and the four lower bits of port 2 belong to group 1. When port 0 is in mode 1 or 2, port 0 and the 5 upper bits of port 2 belong to group 0 and port 1 and the three lower bits of port 2 belong to group 1.

Command Register

The host writes command words to the μPD71055 in this register. These commands control group 0 and group 1. Note that the contents of this register cannot be read.

Group 0 Control and Group 1 Control

These blocks control the operation of group 0 and group 1.

Read/Write Control

The read/write control controls the read/write operations for the ports and the data bus in response to the RD, WR, CS, and address signals. It also handles RESET signals and the A₀, A₁ address inputs.

Data Bus Buffer

The data bus buffer latches information going to or from the system data bus.

Absolute Maximum Ratings

(T_A = 25°C)

Power supply voltage, V _{DD}	-0.5 to +7.0 V
Input voltage, V _I	-0.5 to V _{DD} + 0.3 V
Output voltage, V _O	-0.5 to V _{DD} + 0.3 V
Power dissipation, P _D MAX	500 mW
Operating temperature, T _{opt}	-40 to +85°C
Storage temperature, T _{stg}	-65 to +150°C

Comment: These devices are not meant to be operated outside the limits specified above. Exposure to stresses beyond those listed in Absolute Maximum Ratings could cause damage. Exposure to an absolute maximum rating for extended periods may affect reliability.

Capacitance

(T_A = 25°C, V_{DD} = GND = 0 V)

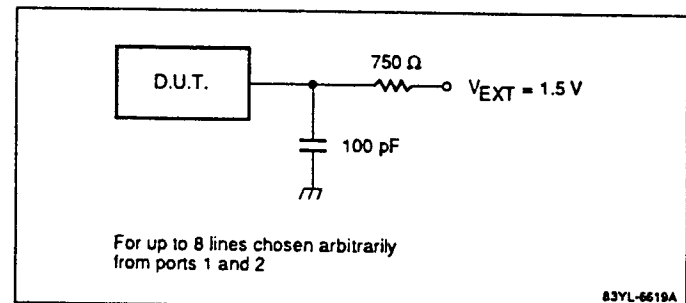
Parameter	Symbol	Limits			Units	Test Conditions
		Min	Typ	Max		
Input capacitance	C _I		10		pF	f _c = 1 MHz Unmeasured pins returned to 0 V
I/O capacitance	C _{I/O}		20		pF	

DC Characteristics

(T_A = -40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Limits			Units	Test Conditions
		Min	Typ	Max		
Input voltage high	V _{IH}	2.2		V _{DD} + 0.3	V	
Input voltage low	V _{IL}	-0.5		0.8	V	
Output voltage high	V _{OH}	0.7 V _{DD}			V	I _{OH} = -400 μA
Output voltage low	V _{OL}			0.4	V	I _{OL} = 2.5 mA
Darlington drive current	I _{DAR}	-1.0		-4.0	mA	See test setup diagram
Input leakage current high	I _{LIH}			10	μA	V _I = V _{DD}
Input leakage current low	I _{LIL}			-10	μA	V _I = 0 V
Output leakage current high	I _{LOH}			10	μA	V _O = V _{DD}
Output leakage current low	I _{LOL}			-10	μA	V _O = 0 V
Supply current (dynamic)						
μPD71055	I _{DD1}			10	mA	Normal operation
μPD71055-10	I _{DD1}		5	10	mA	Normal operation
Supply current (standby)	I _{DD2}		2	50	μA	Inputs: RESET = 0.1 V, others = V _{DD} - 0.1 V Outputs: Open

Test Setup for I_{DAR} Measurement



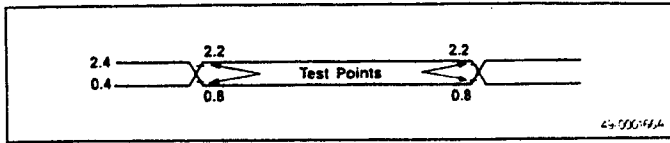
AC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$)

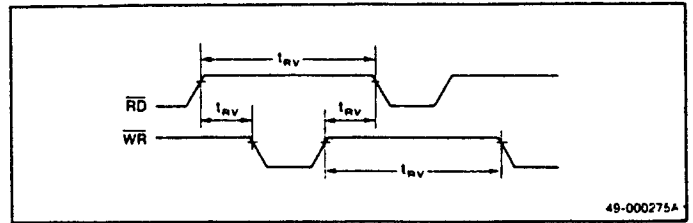
Parameter	Symbol	8 MHz Limits		10 MHz Limits		Unit	Test Conditions
		Min	Max	Min	Max		
Read Timing							
$A_1, A_0, \overline{\text{CS}}$ set-up to $\overline{\text{RD}} \downarrow$	t_{SAR}	0		0		ns	
$A_1, A_0, \overline{\text{CS}}$ hold from $\overline{\text{RD}} \uparrow$	t_{HRA}	0		0		ns	
$\overline{\text{RD}}$ pulse width	t_{RRL}	160		150		ns	
Data delay from $\overline{\text{RD}} \downarrow$	t_{DRD}		120		100	ns	$C_L = 150\text{ pF}$
Data float from $\overline{\text{RD}} \uparrow$	t_{FRD}	10	85	10	60	ns	$C_L = 20\text{ pF}; R_L = 2\text{ k}\Omega$
Read recovery time	t_{RV}	200		150		ns	
Write Timing							
$A_1, A_0, \overline{\text{CS}}$ set-up to $\overline{\text{WR}} \downarrow$	t_{SAW}	0		0		ns	
$A_1, A_0, \overline{\text{CS}}$ hold from $\overline{\text{WR}} \uparrow$	t_{HWA}	0		0		ns	
$\overline{\text{WR}}$ pulse width	t_{WWL}	120		100		ns	
Data set-up to $\overline{\text{WR}} \uparrow$	t_{SDW}	100		100		ns	
Data hold from $\overline{\text{WR}} \uparrow$	t_{HWD}	0		0		ns	
Write recovery time	t_{RV}	200		150		ns	
Other Timing							
Port set-up time to $\overline{\text{RD}} \downarrow$	t_{SPR}	0		0		ns	
Port hold time from $\overline{\text{RD}} \uparrow$	t_{HRP}	0		0		ns	
Port set-up time to $\overline{\text{STB}} \downarrow$	t_{SPS}	0		0		ns	
Port hold time from $\overline{\text{STB}} \uparrow$	t_{HSP}	150		150		ns	
Port delay time from $\overline{\text{WR}} \uparrow$	t_{DWP}		350		200	ns	$C_L = 150\text{ pF}$
$\overline{\text{STB}}$ pulse width	t_{SSL}	350		100		ns	
$\overline{\text{DAK}}$ pulse width	t_{DADAL}	300		100		ns	
Port delay time from $\overline{\text{DAK}} \downarrow$ (mode 2)	t_{DDAP}		300		150	ns	$C_L = 150\text{ pF}$
Port float time from $\overline{\text{DAK}} \uparrow$ (mode 2)	t_{FDAP}	20	250	20	250	ns	$C_L = 20\text{ pF}; R_L = 2\text{ k}\Omega$
$\overline{\text{OBF}}$ set delay from $\overline{\text{WR}} \uparrow$	t_{DWOB}		300		150	ns	$C_L = 150\text{ pF}$
$\overline{\text{OBF}}$ clear delay from $\overline{\text{DAK}} \downarrow$	t_{DDAOB}		350		150	ns	
IBF set delay from $\overline{\text{STB}} \downarrow$	t_{DSIB}		300		150	ns	
IBF clear delay from $\overline{\text{RD}} \uparrow$	t_{DRIB}		300		150	ns	
INT set delay from $\overline{\text{DAK}} \uparrow$	t_{DDAI}		350		150	ns	
INT clear delay from $\overline{\text{WR}} \downarrow$	t_{DWI}		450		200	ns	
INT set delay from $\overline{\text{STB}} \uparrow$	t_{DSI}		300		150	ns	
INT clear delay from $\overline{\text{RD}} \downarrow$	t_{DRI}		400		200	ns	
RESET pulse width	t_{RESET1}	50		50		μs	During right after power-on
	t_{RESET2}	500		500		ns	During operation

Timing Waveforms

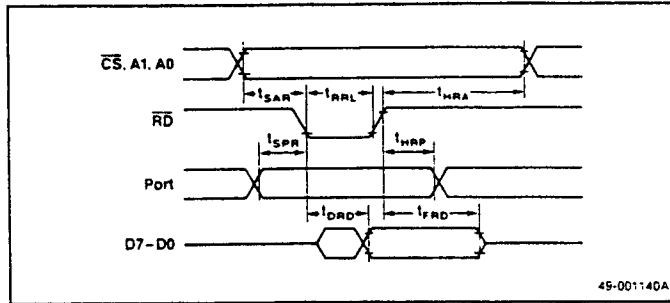
AC Test Waveform



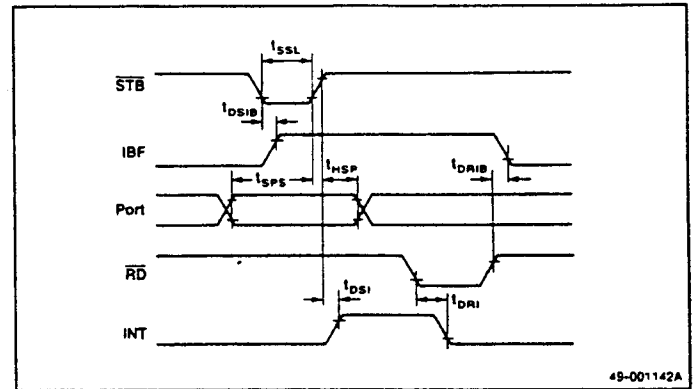
Recovery Time



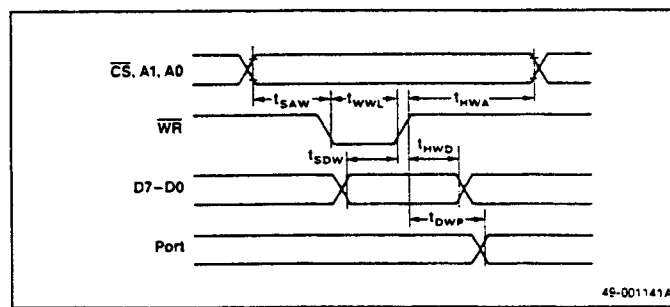
Timing Mode 0: Input



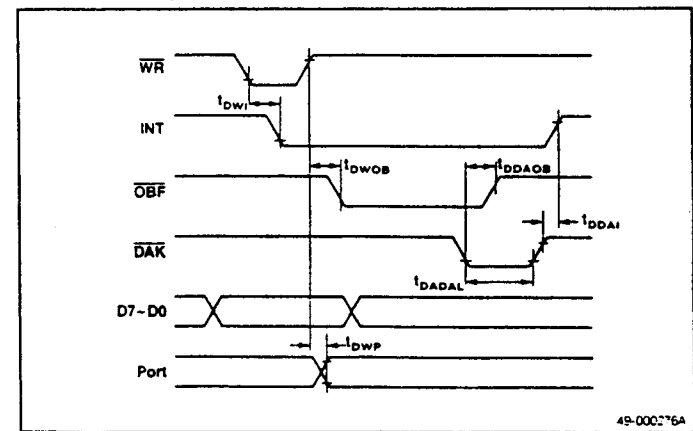
Mode 1: Input



Mode 0: Output

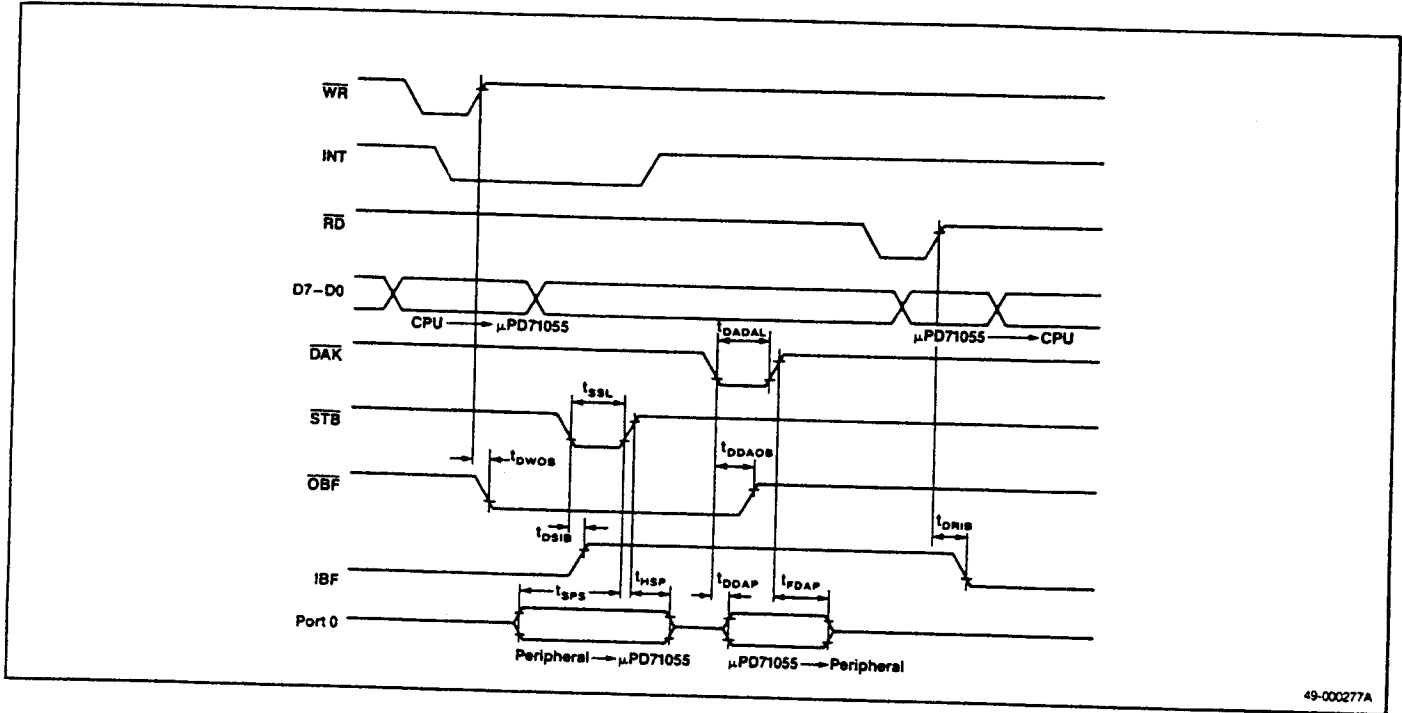


Mode 1: Output



Timing Waveforms (cont)

Mode 2



49-000277A

μ PD71055 Commands

Two commands control μ PD71055 operation. The mode select command determines the operation of group 0 and group 1 ports. The bit manipulation command sets or resets the bits of port 2. These commands are executed by writing an 8-bit command word to the command register ($A_1A_0 = 11$).

Mode Select

The μ PD71055 port groups have three modes. Modes 0 and 1 can be specified for groups 0 and 1, but mode 2 can only be specified for group 0. The bits of all ports are cleared when a mode is selected or when the μ PD71055 is reset.

Mode 0. Basic input/output port operation.

Mode 1. Strobed input/output operation controlled by three or four bits of port 2 used as control/status signals.

Mode 2. (Only available for group 0). Port 0 is the bidirectional I/O port and the higher 5 bits of port 2 are used for status and control signals.

To specify the mode, set the command word as shown in figure 1 and write it to the command register.

Bit Manipulation Command

This command (figure 2) affects only port 2. It is mainly used in mode 1 and mode 2 to control the port 2 bits which are used as control/status signals. It is also used to enable and disable μ PD71055-generated interrupts and to set and reset port 2 general input/output pins.

For example, to set bit 2 of port 2 to 1 ($P2_2 = 1$), set the command word as shown in figure 3 (05H) in the command register.

Operation in Each Mode

The operation mode for each group in the μ PD71055 can be set according to the application. Group 0 can be in modes 0, 1, or 2, while group 1 is in mode 0 or 1. Group 1 cannot be used in mode 2.

The \overline{RD} and \overline{WR} signals that appear in the descriptions of each mode refer to the port in question as addressed by A_1 and A_0 . These signals only affect the port addressed by A_1 and A_0 .

Where the port addressed may not be clear, 0 or 1 is appended to the signal name to indicate the port.

Mode 0

In this mode the ports of the μ PD71055 are used to perform basic I/O operations. Each port operates with a buffered input and a buffered latched output. See figure 4.

Depending on the control word sent to the μ PD71055 from the system bus, ports 0, 1, and 2 can be independently specified for input or output.

Input Port Operation

While the \overline{RD} signal is low, data from the port selected by the A_1A_0 signals is put on the data bus. See figure 5.

Output Port Operation

When the μ PD71055 is written to ($\overline{WR} = 0$), the data on the data bus will be latched in the port selected by the A_1A_0 signals at the rising edge of \overline{WR} and output to the port pins (figure 6). Following the programming of mode 0, all outputs are at a low level.

By reading a port which is set for output, the output value of the port can be obtained.

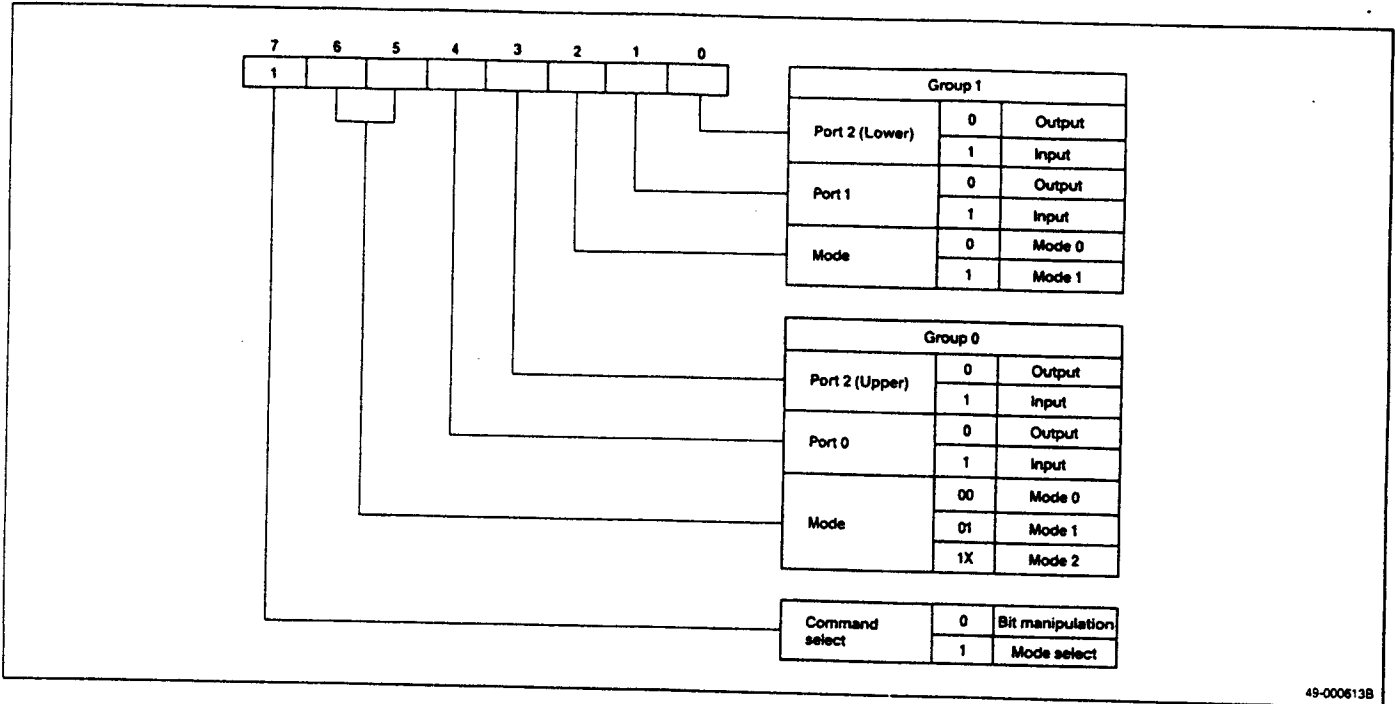
Note: When group 0 is in mode 1 or mode 2, only bits $P2_2$ - $P2_0$ of port 2 can be used by group 1. Bit $P2_3$ belongs to group 0.

Mode 0 Example

This is an example of a CPU connected to an A/D converter via a μ PD71055 (figure 7). Here both group 0 and group 1 are set to mode 0 and port 2 is used to start conversion and detect the end of the conversion process.

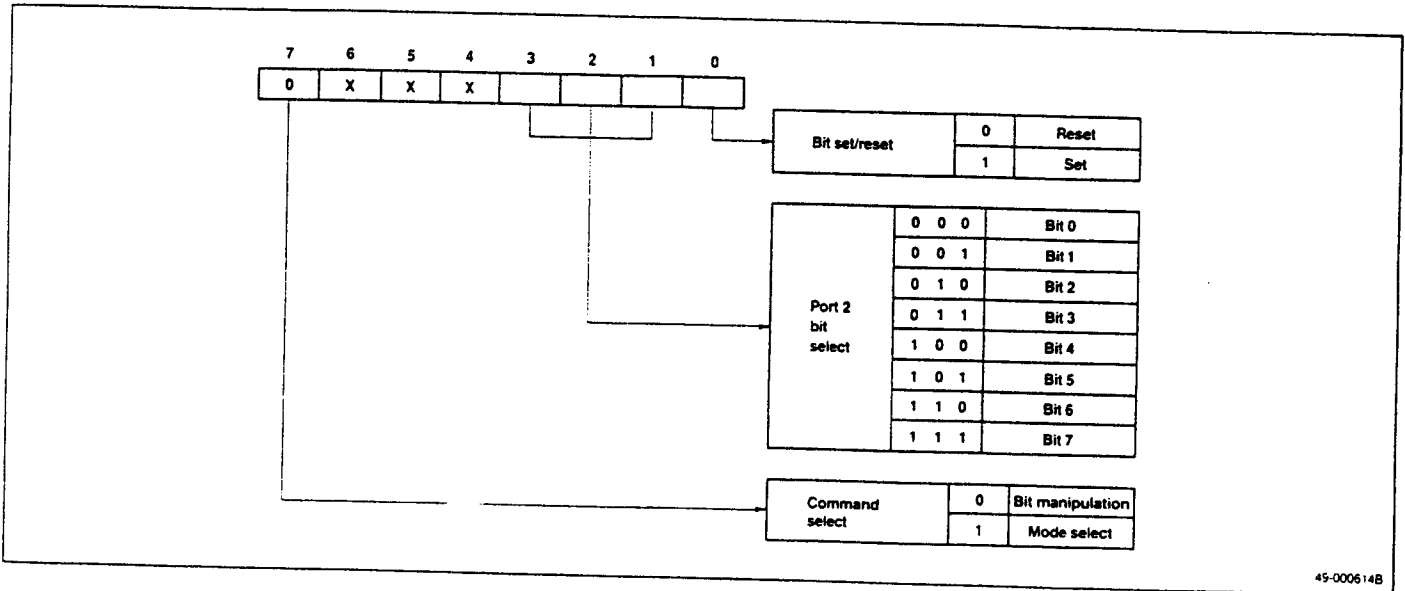
Figure 8 is a subroutine that reads the converted data from an A/D converter.

Figure 1. Mode Select Command Word



49-000613B

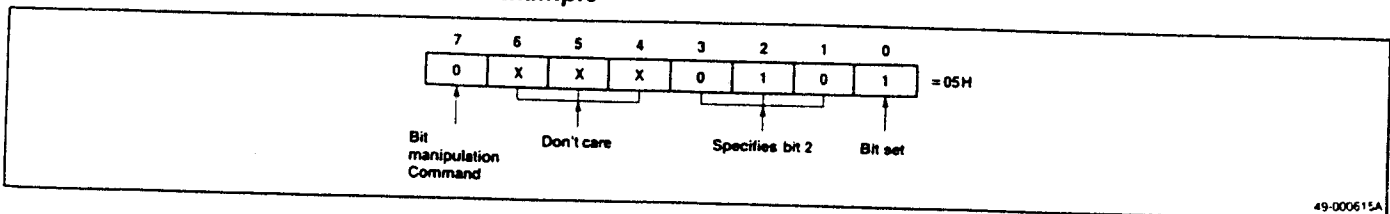
Figure 2. Bit Manipulation Command Word



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49-000614B

Figure 3. Bit Manipulation Command Example



49-000615A

Figure 4. Mode 0

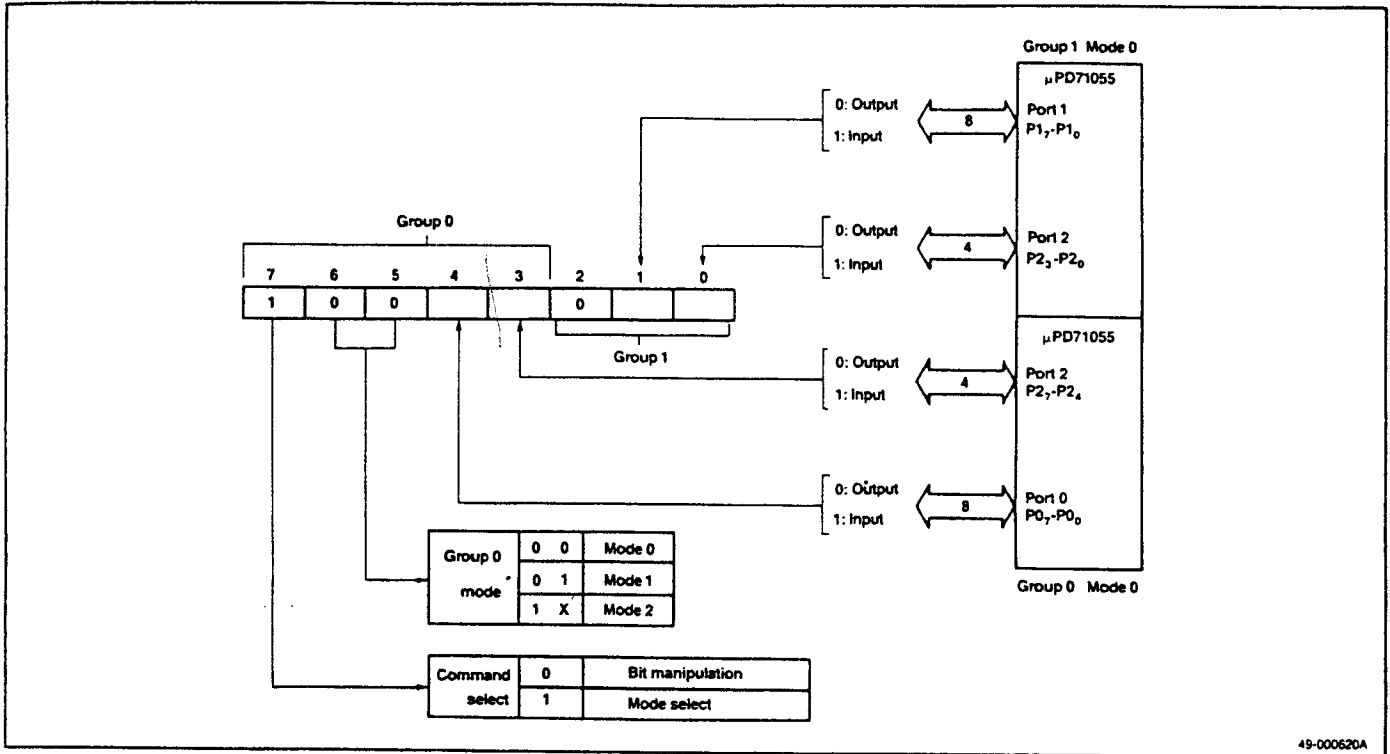


Figure 5. Mode 0 Input Timing

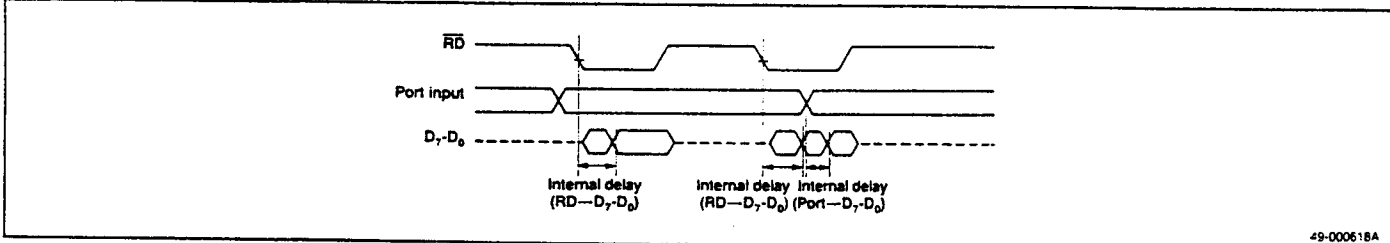


Figure 6. Mode 0 Output Timing

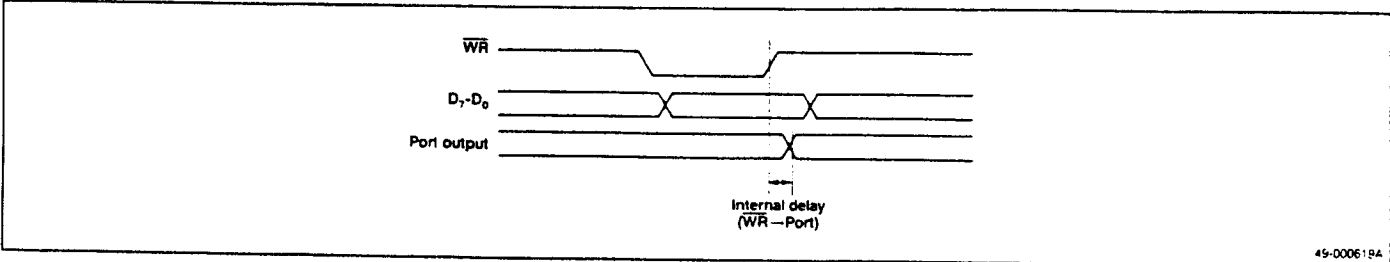


Figure 7. A/D Converter Connection Example

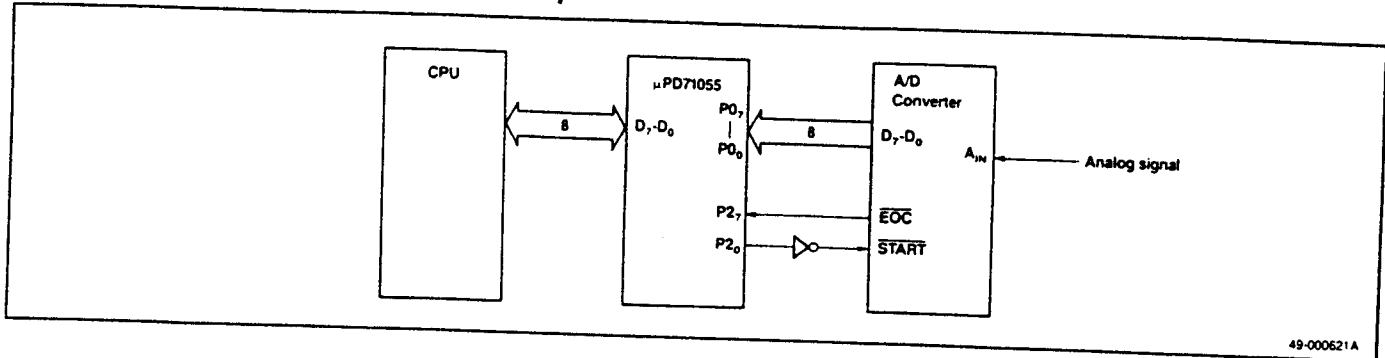


Figure 8. A/D Converter Example

```

READ_A/D:  MOV     AL,10011000B           ;μPD71055 Mode Setting:
           OUT     CTRLPORT,AL          ;Group 0, group 1 in mode 0
                                           ;Port 0 & port 2 (upper) are inputs
                                           ;Port 1 & port 2 (lower) are outputs

           MOV     AL,00000001B
           OUT     CTRLPORT,AL          ;Conversion starts by setting P20 high
WAIT_EOC:  IN      AL,PORT2              ;End of conversion wait loop
           TEST1   AL,7                  ;Conversion ends when P27 = 0
           BNZ    WAIT_EOC
           IN      AL,PORT0              ;Read A/D converted values
           RET
    
```

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Mode 1

In this mode, the control and status signals control the I/O data. In group 0, port 0 functions as the data port and the upper five bits of port 2 function as control/status. In group 1, port 1 functions as the data port and the lower three bits of port 2 function as control/status.

In mode 1, the bit manipulation command is used to write the bits of port 2.

Group 0 Mode 1

When group 0 is used in mode 1, the upper five bits of port 2 become part of group 0. Of these five bits, three are used for control/status and the remaining two can be used for I/O (using the bit manipulation command). See figure 9.

Group 1 Mode 1

When group 1 is used in mode 1, the lower three or four bits of port 2 become part of group 1. Of these four bits, three are used for control/status. The remaining bit, P2₃, can be used for I/O only if group 0 is in mode 0. Otherwise, P2₃ belongs to group 0 as a control/status bit. See figure 9 and table 4.

Mode 1 Input Operation

In mode 1, port 0 is the data port for group 0, and port 1 for group 1. The control/status bits (port 2) are used as listed below. Figure 10 shows the signal timing.

STB [Strobe]. The data input at port 0 is latched in port 0 when the $\overline{STB0}$ input is brought low. The data input at port 1 is latched in port 1 by $\overline{STB1}$.

IBF [Input Buffer Full F/F]. The IBF output goes high to indicate that the input buffer has become full. IBF goes high when the \overline{STB} signal goes low. IBF goes low at the rising edge of the \overline{RD} signal when $\overline{STB} = 1$.

The IBF F/F is cleared when mode 1 is programmed.

INT [Interrupt Request]. INT goes high when the data is latched in the input port, when RIE is 1 and \overline{STB} , IBF and \overline{RD} are all high. INT goes low at the falling edge of the \overline{RD} signal. It can function as a data read request interrupt signal to a CPU.

INT is cleared when mode 1 is programmed.

Figure 9. Mode 1 Input

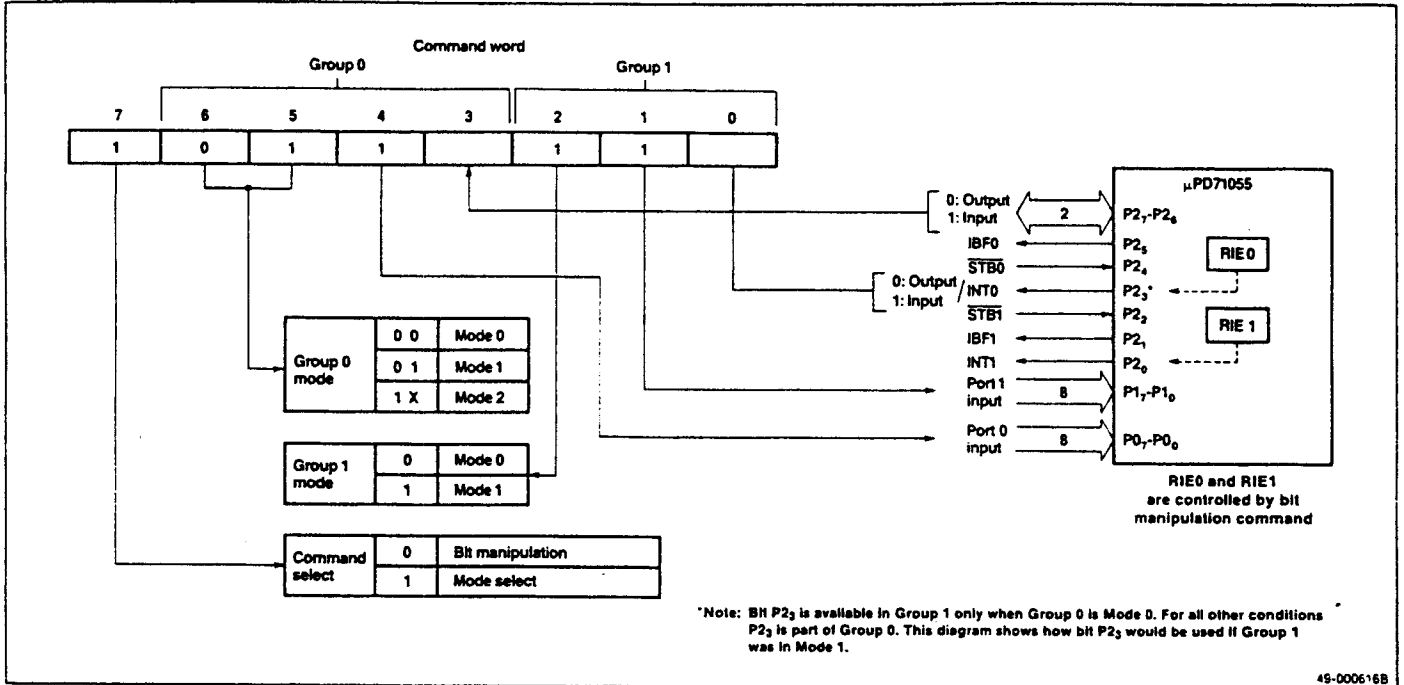
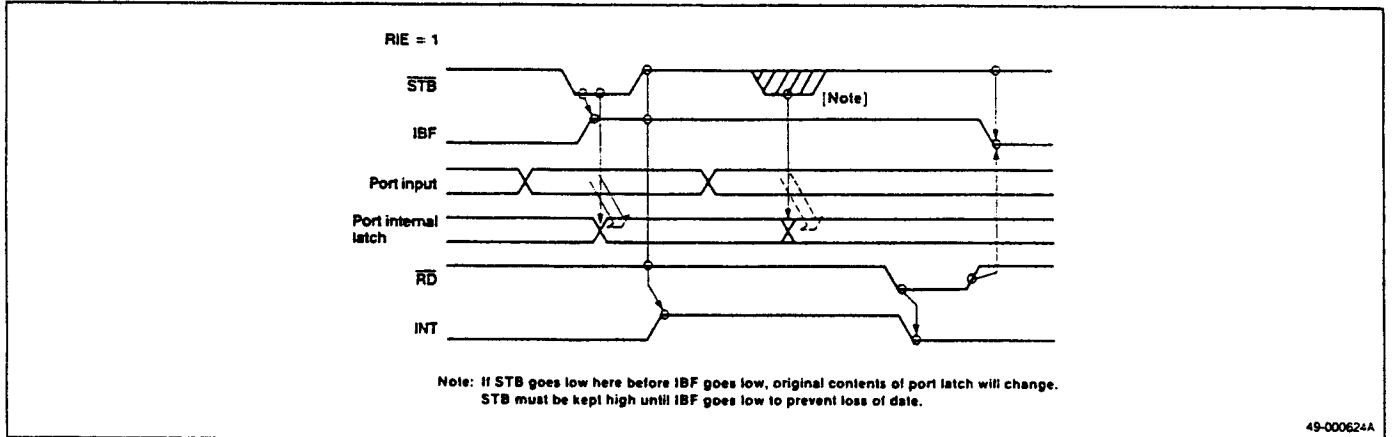


Figure 10. Mode 1 Input Timing



RIE [Read Interrupt Enable Flag]. RIE controls the interrupt output. Interrupts can be enabled by using the bit manipulation command to set this bit to 1, and disabled by resetting it to 0. This signal is internal to the μPD71055 and is not an output. The state of RIE does not affect the function of $\overline{STB0}$ or $\overline{STB1}$, which are inputs to the same bits (P2₄ and P2₂) of port 2.

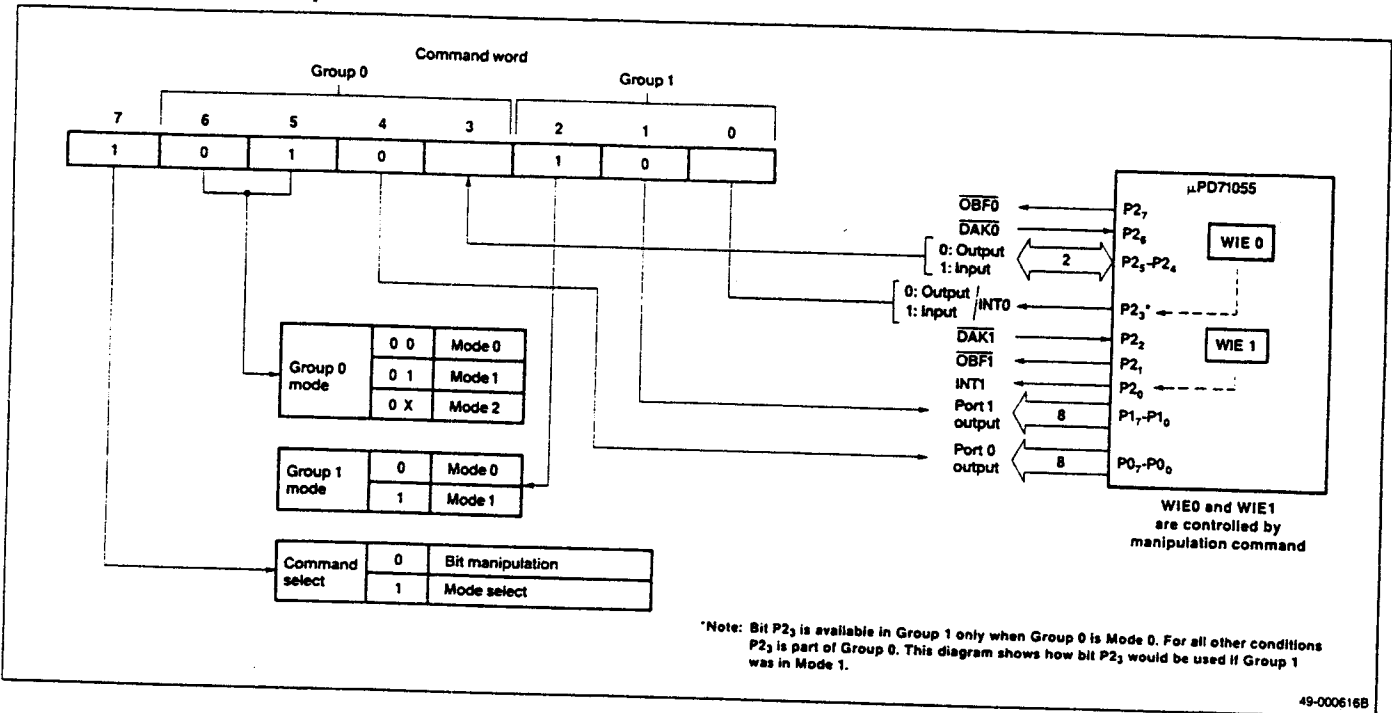
When input is specified in mode 1, the status of IBF, INT and RIE can be read by reading the contents of port 2.

Mode 1 Output Operation

In mode 1 output operation (figure 11), the status/control bits (port 2) are used as listed below. Figure 12 shows the signal timing.

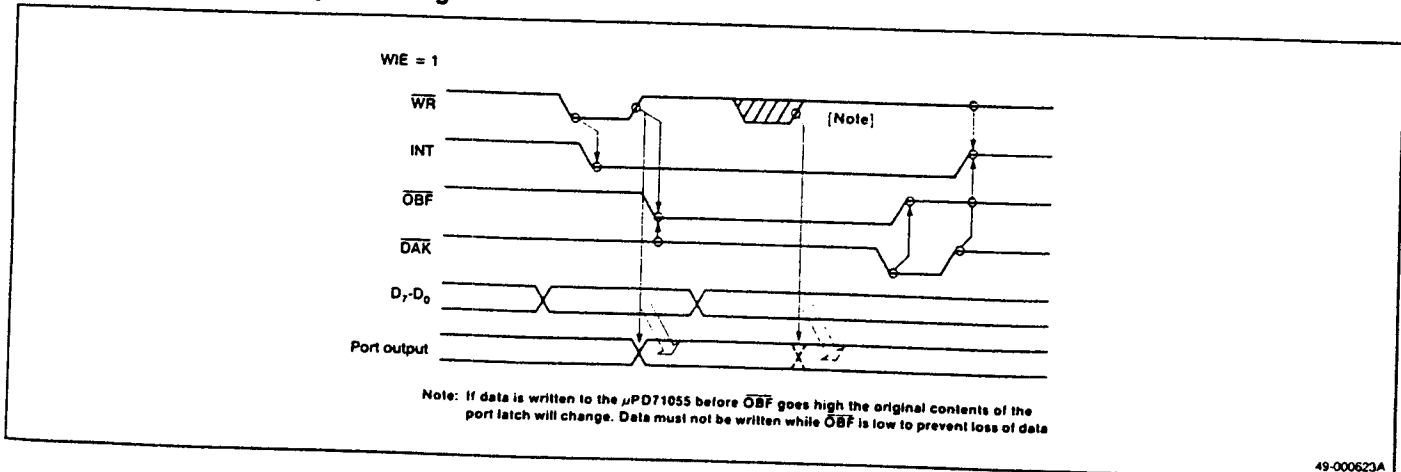
\overline{OBF} [Output Buffer Full F/F]. \overline{OBF} goes low when data is received by the μPD71055 and is latched in output ports 1 or 0. \overline{OBF} functions as a data receive flag. \overline{OBF} goes low at the rising edge of \overline{WR} when $\overline{DAK} = 1$ (write complete). It goes high when the \overline{DAK} signal goes low.

Figure 11. Mode 1 Output



*Note: Bit P2₃ is available in Group 1 only when Group 0 is Mode 0. For all other conditions P2₃ is part of Group 0. This diagram shows how bit P2₃ would be used if Group 1 was in Mode 1.

Figure 12. Mode 1 Output Timing



DAK [Data Acknowledge]. When this input is low, it signals the μPD71055 that output port data has been taken from the 71055.

INT [Interrupt Request]. INT goes high when the output data is taken when WIE is set to 1 and \overline{WR} , \overline{OBF} and \overline{DAK} are all high. It goes low at the falling edge of the \overline{WR} signal. INT therefore functions as a write request signal, indicating that new data should be sent to the μPD71055.

WIE [Write Interrupt Enable Flag]. WIE controls the interrupt output. Interrupts can be enabled by using the bit manipulation command to set this bit to 1 and disabled by resetting it to 0. This signal is internal to the μPD71055 and is not an output. The state of WIE does not affect the function of \overline{DAK} addressed to the same bits of port 2.

When output is specified in mode 1, the status of \overline{OBF} , INT and WIE can be obtained by reading the contents of port 2.

Table 2 shows a summary of these signals.

Table 2. Functions of Port 2 Bits in Mode 1

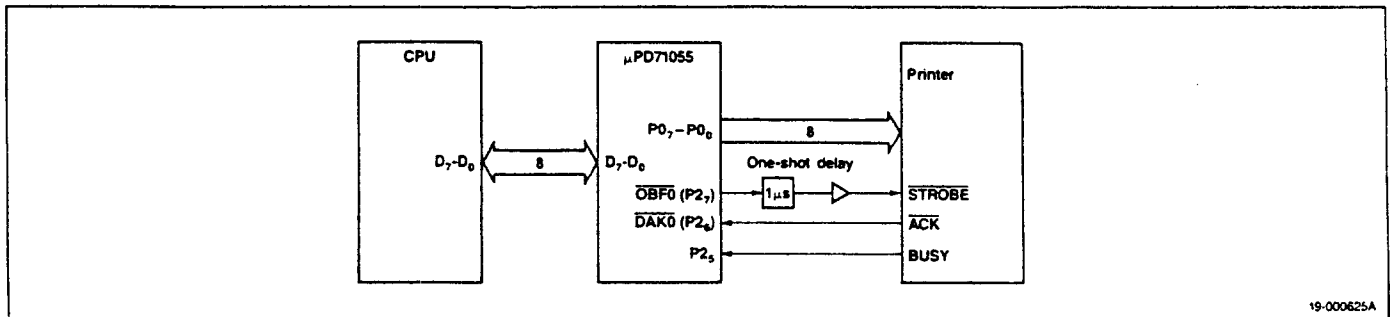
Group	Bit	Data Input	Data Output
1	P2 ₀	INT1 (Interrupt request)	INT1 (Interrupt request)
	P2 ₁	IBF1 (Input buffer full 1/1)	\overline{OBF} 1 (Output buffer full 1/1)
	P2 ₂	STB1 (Strobe input)	DAK1 (Data acknowledge input)
		RIE1 (Read interrupt enable flag)	WIE1 (Write interrupt enable flag)
P2 ₃	I/O (Note)	I/O (Note)	
0	P2 ₃	INT0 (Interrupt request)	INT0 (Interrupt request)
	P2 ₄	STB0 (Strobe input)	I/O
		RIE0 (Read interrupt enable flag)	
	P2 ₅	IBF0 (Input buffer full 1/1)	I/O
	P2 ₆	I/O	DAK0 (Data acknowledge input)
			WIE0 (Write interrupt enable flag)
P2 ₇	I/O	\overline{OBF} 0 (Output buffer full 1/1)	

Note: Can be used with group 1 only when group 0 is set to mode 0. In other modes, P2₃ belongs to group 0.

Mode 1 Example

This example (figure 13) demonstrates connecting a printer to the μPD71055. Group 0 is used in mode 1 output. Group 1 can operate in mode 0 or 1; in this example it is set to mode 0.

Figure 13. Connection to Printer



19-000625A

Figure 14. Printer Example Subroutine

```

;This subroutine sends character strings to the printer
INIT:      MOV      AL,10101000B      ;μPD71055 Mode Setting:
                                           ;Group 0: mode 1 output
                                           ;Group 1: mode 0

                OUT      CTRLPORT,AL
                RET
SENDPRN:   MOV      BW,DATA          ;Output data address
PRNLOOP:   MOV      AL,[BW]
                CMP      AL,0FFH      ;End if data = 0FFH
                BNZ      WAIT
                RET
WAIT:      IN       AL,PORT2
                TEST1   AL,7          ;Wait until output buffer is empty
                BZ      WAIT
                TEST1   AL,5          ;Wait until printer can accept data
                BNZ      WAIT
                MOV      AL,[BW]      ;Send data to printer
                OUT      PORT0,AL
                INC      BW
                BR      PRNLOOP
    
```

Mode 2

Mode 2 can only be used by group 0. In this mode, port 0 functions as a bidirectional 8-bit data port operating under the control of the upper five bits of port 2 as control/status signals. In this mode, port 0 combines the input and output operations of mode 1. See figures 15 and 16.

In mode 2, the status of the following signals can be determined by reading port 2: $\overline{\text{OBF0}}$, IBF0 , INT0 , WIE0 , and RIE0 .

The $\overline{\text{DAK0}}$ and $\overline{\text{STB0}}$ signals are used to select input or output for port 0. By using these signals, bidirectional operation between the μPD71055 and peripheral can be realized.

In mode 2, the bit manipulation command is used to write to port 2.

Control/Status Port Operation

The following control/status signals are used for output:

$\overline{\text{OBF0}}$ [Output Buffer Full]. $\overline{\text{OBF0}}$ goes low when data is received from the $\text{D}_0\text{-D}_7$ data bus and is latched in the port 0 output buffer. It therefore functions as a receive request signal to the peripheral. $\overline{\text{OBF0}}$ goes low

at the rising edge of the $\overline{\text{WR0}}$ signal (end of data write). It goes high when $\overline{\text{DAK0}}$ is low (output data from port 0 received).

$\overline{\text{DAK0}}$ [Data Acknowledge]. $\overline{\text{DAK0}}$ is sent to the μPD71055 in response to the $\overline{\text{OBF0}}$ signal. It should be set low when data is received from port 0 of the μPD71055.

WIE0 [Write Interrupt Enable Flag]. WIE0 controls the write interrupt request output. Interrupts are enabled by using the bit manipulation command to set this bit to 1 and disabled by setting it to 0. The state of WIE does not affect the $\overline{\text{DAK}}$ function of this pin.

The following control/status signals are used for input:

$\overline{\text{STB0}}$ [Strobe Input]. When $\overline{\text{STB0}}$ goes low, the data being sent to the μPD71055 is latched in port 0.

IBF0 [Input Buffer Full F/F]. When IBF0 goes high, it indicates that the input buffer is full. It functions as a signal which can be used to prohibit further data transfer. IBF0 goes high when $\overline{\text{STB0}}$ goes low. It goes low at the rising edge of $\overline{\text{RD0}}$ when $\overline{\text{STB0}} = 1$ (read complete).

Figure 15. Mode 2

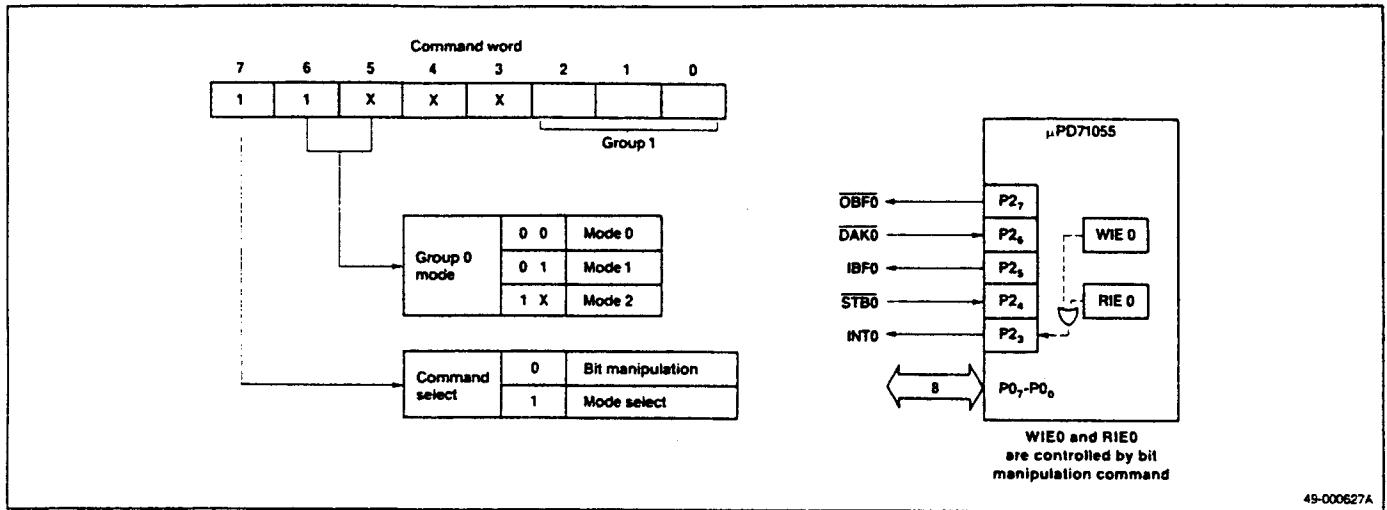
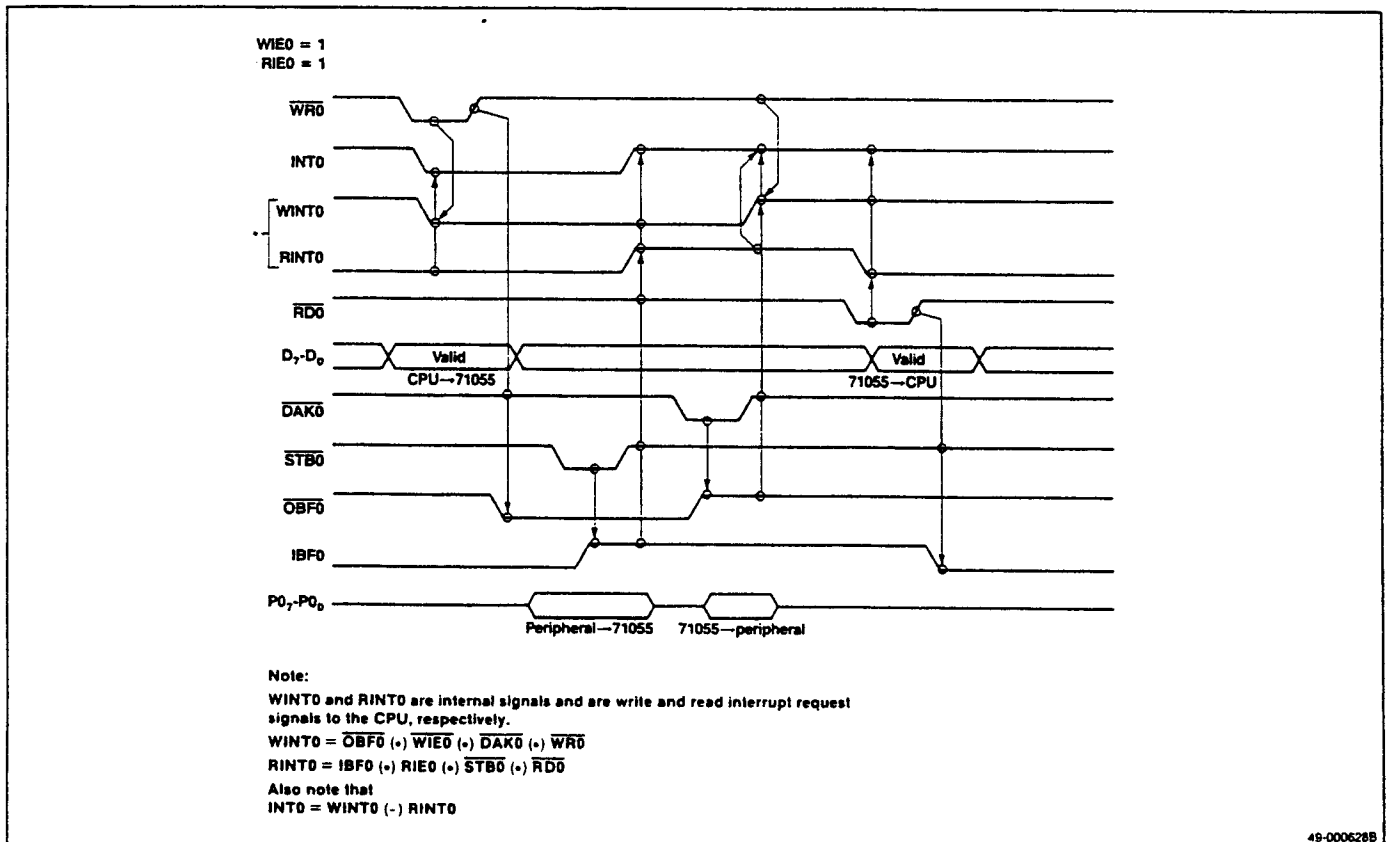


Figure 16. Mode 2 Timing



RIE0 [Read Interrupt Enable Flag]. RIE0 controls the read interrupt request output. Interrupts are enabled by using the bit manipulation command to set this bit to 1 and disabled by setting it to 0. The state of RIE0 does not affect the $\overline{STB0}$ function of this pin.

This control/status signal is used for both input and output:

INT0 [Interrupt Request]. During input operations, INT0 functions as a read request interrupt signal. During output, it functions as a write request interrupt signal. This signal is the logical OR of the INT signal for data read (RINT0) and the INT signal for write (WINT0) in mode 1 (RINT0 OR WINT0).

In mode 2, the status of $\overline{OBF0}$, IBF0, INT0, WIE0, and RIE0 can be determined by reading port 2.

Table 3 is a summary of these signals.

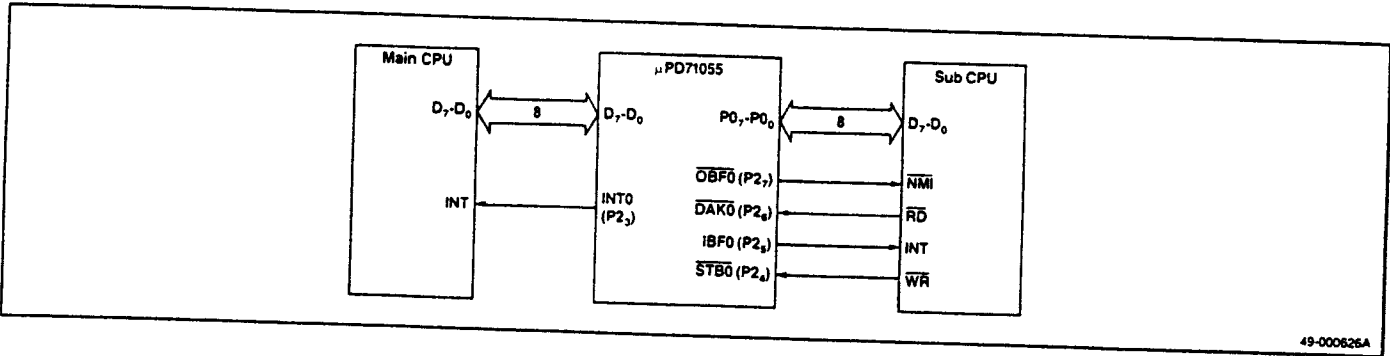
Table 3. Functions of Port 2 in Mode 2

Bit	Function
P2 ₃	INT0 (Interrupt request)
P2 ₄	$\overline{STB0}$ (Strobe input) RIE0 (Read interrupt enable flag)
P2 ₅	IBF0 (Input buffer full f/f)
P2 ₆	$\overline{DAK0}$ (Data acknowledge input) WIE0 (Write interrupt enable flag)
P2 ₇	$\overline{OBF0}$ (Output buffer full f/f)

Mode 2 Example

Figures 17, 18, and 19 show data transfer between two CPUs.

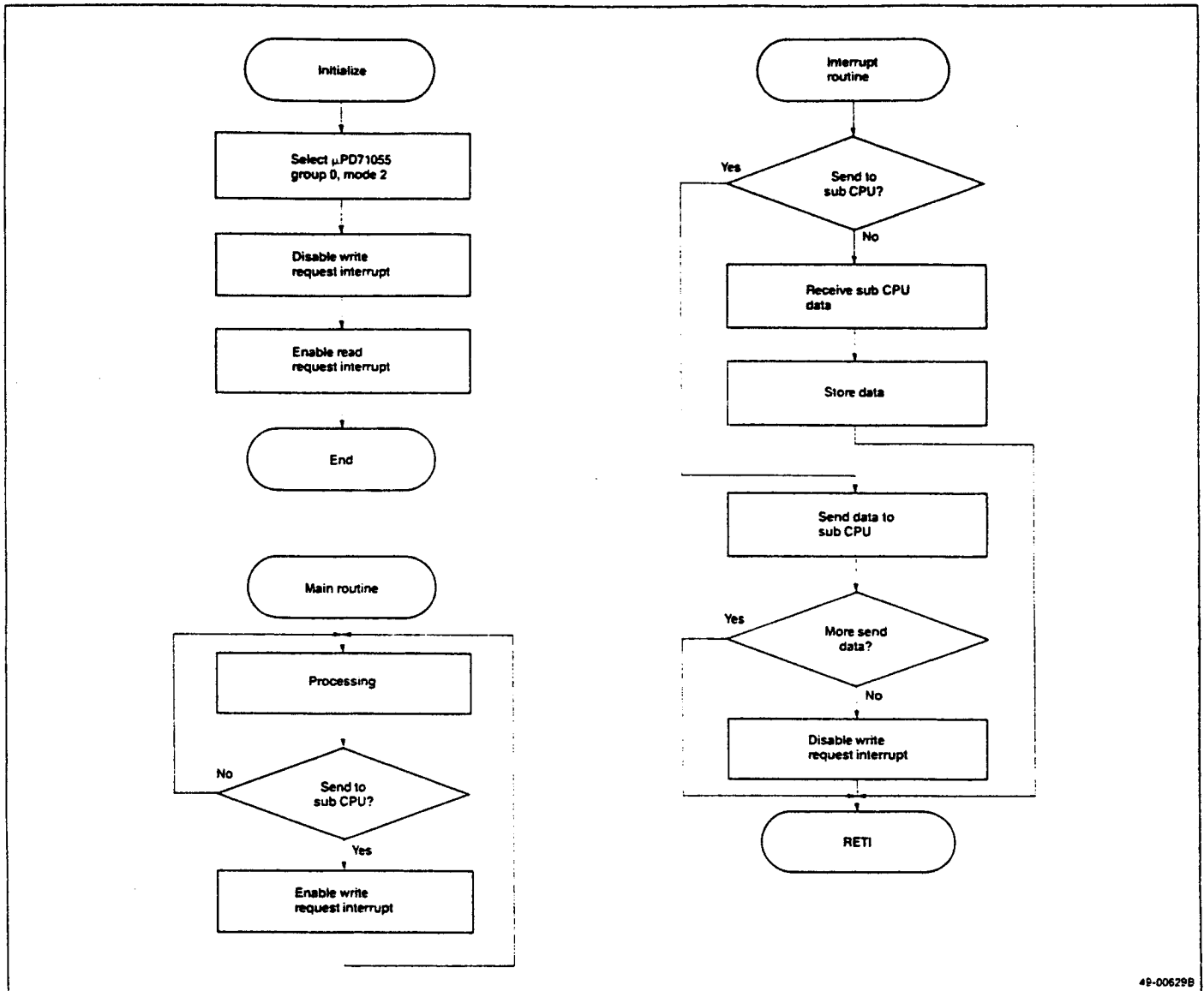
Figure 17. Connecting Two CPUs



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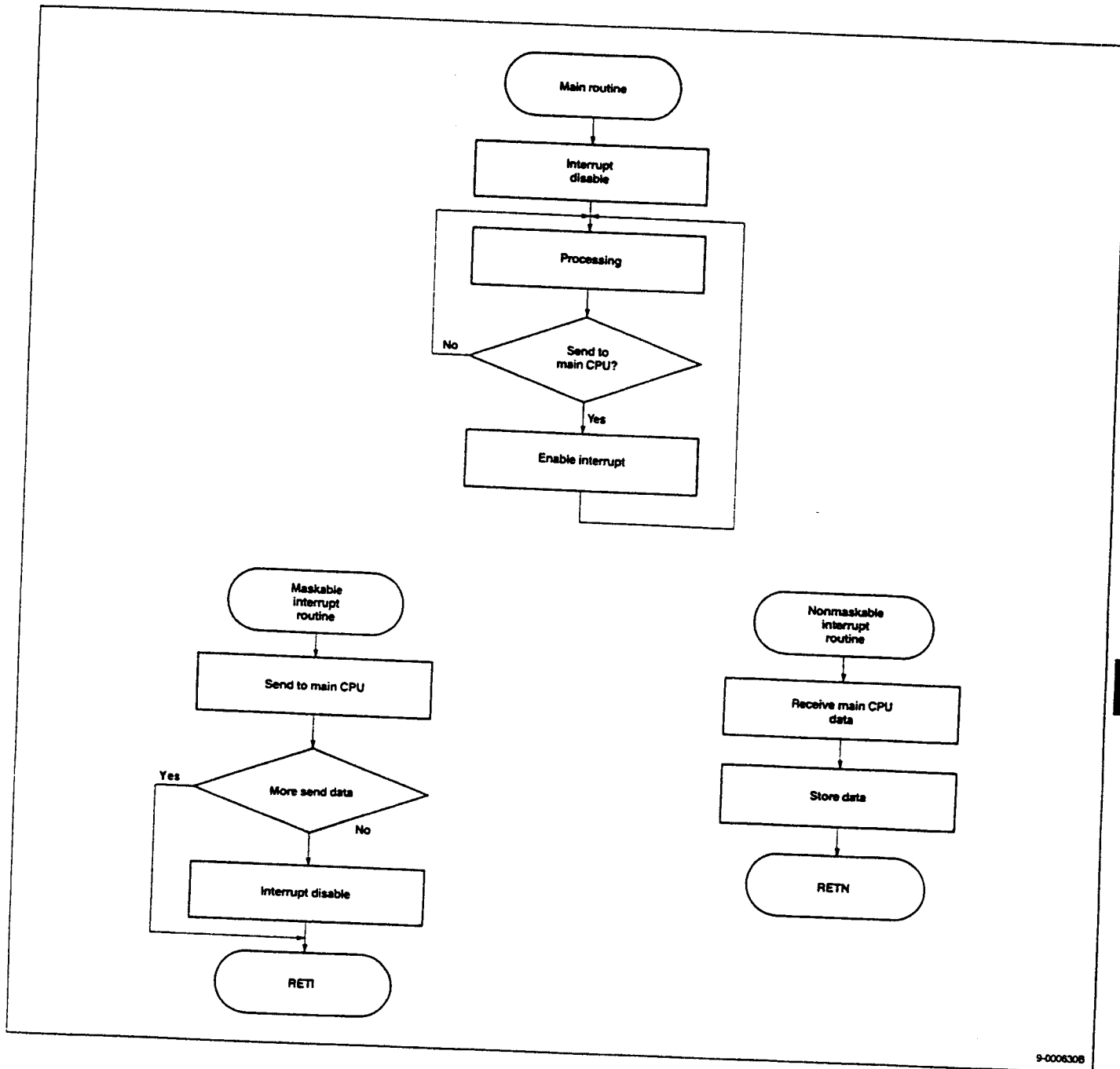
49-000626A

Figure 18. Main CPU Flowchart



4P-00629B

Figure 19. Sub CPU Flowchart



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Mode Combinations

Table 4 is a complete list of all the combinations of modes and groups, and the function of the port 2 bits in each mode.

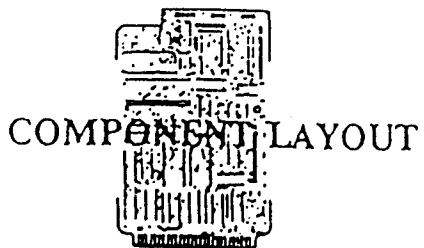
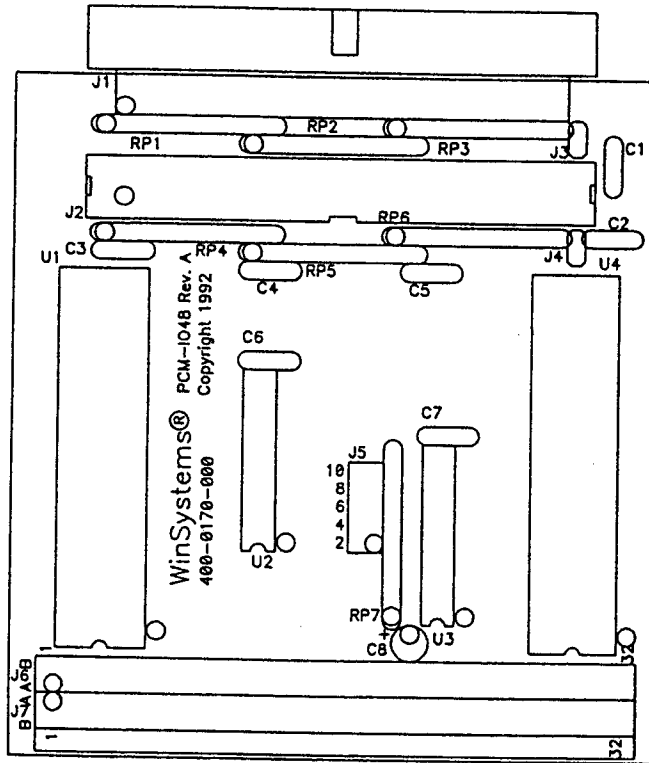
Table 4. Mode Combinations and Port 2 Bit Functions

Mode	Group 0						Mode	Group 1				
	P0 ₇ -P0 ₀	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃		P1 ₇ -P1 ₀	P2 ₃	P2 ₂	P2 ₁	P2 ₀
0	In	D	D	D	D	NA	0	In	D	D	D	D
0	In	D	D	D	D	NA	0	Out	D	D	D	D
0	In	D	D	D	D	NA	1	In	B	STB1 (RIE1)	IBF1	INT1
0	In	D	D	D	D	NA	1	Out	B	DAK1 (WIE1)	OBF1	INT1
0	Out	D	D	D	D	NA	0	In	D	D	D	D
0	Out	D	D	D	D	NA	0	Out	D	D	D	D
0	Out	D	D	D	D	NA	1	In	B	STB1 (RIE1)	IBF1	INT1
0	Out	D	D	D	D	NA	1	Out	B	DAK1 (WIE1)	OBF1	INT1
1	In	B	B	IBF0	STB0 (RIE0)	INT0	0	In	NA	D	D	D
1	In	B	B	IBF0	STB0 (RIE0)	INT0	0	Out	NA	D	D	D
1	In	B	B	IBF0	STB0 (RIE0)	INT0	1	In	NA	STB1 (RIE1)	IBF1	INT1
1	In	B	B	IBF0	STB0 (RIE0)	INT0	1	Out	NA	DAK1 (WIE1)	OBF1	INT1
1	Out	OBF0	DAK0 (WIE0)	B	B	INT0	0	In	NA	D	D	D
1	Out	OBF0	DAK0 (WIE0)	B	B	INT0	0	Out	NA	D	D	D
1	Out	OBF0	DAK0 (WIE0)	B	B	INT0	1	In	NA	STB1 (RIE1)	IBF1	INT1
1	Out	OBF0	DAK0 (WIE0)	B	B	INT0	1	Out	NA	DAK1 (WIE1)	OBF1	INT1
2	I/O	OBF0	DAK0 (WIE0)	IBF0	STB0 (RIE0)	INT0	0	In	NA	D	D	D
2	I/O	OBF0	DAK0 (WIE0)	IBF0	STB0 (RIE0)	INT0	0	Out	NA	D	D	D
2	I/O	OBF0	DAK0 (WIE0)	IBF0	STB0 (RIE0)	INT0	1	In	NA	STB1 (RIE1)	IBF1	INT1
2	I/O	OBF0	DAK0 (WIE0)	IBF0	STB0 (RIE0)	INT0	1	Out	NA	DAK1 (WIE1)	OBF1	INT1

Note:

- (1) In this chart, "NA" indicates that the bit cannot be used by this group.
- (2) The symbol "B" indicates bits that can only be rewritten by the bit manipulation command.
- (3) In this chart, "D" indicates that is used by the user.
- (4) Symbols in parentheses are internal flags. They are not output to port 2 pins and they cannot be read by the host.
- (5) In indicates Input, Out indicates Output, and I/O indicates Input/Output.

PCM-1048 Parts Placement



COMPONENT LAYOUT

BEGINNING RANGE: PCM-1048

ENDING RANGE: PCM-1048

EVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	PCM-1048	PC/104 48 LINE DIGITAL I/O, 8-BIT					1
2	999-9999-001	SPECIAL NOTES	01-25-93 RC RELEASED	ARLIN		Inv	1
2	0170-100-0000	ASSY PCM-1048 REV A	ASSY PCM-1048 REV A	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	01-25-93 RC RELEASED	ARLIN		Inv	1
3	>110-0010-003	CAP .1 UF CER RAD SR215E104MAA	C1-C7	ARLIN		Inv	7
3	>110-0014-005	CAP 10 UF TAN RAD T350E106K025AS	C8	ARLIN		Inv	1
3	>117-0103-050	RN SIP 10P-9 RES 10K SRDA-10P-C1	RP1-RP7	ARLIN		Inv	7
3	>201-0064-120	HDR RA 2X32 TSW-132-08-G-D-RA	J7	ARLIN		Inv	1
3	>200-0064-100	SOCKET 64 POS STACK AT-ESI-64-12	J13 MUST BE HAND SOLDERED	ARLIN		Inv	1
3	>200-0203-100	SOCKET 20 PIN ICO-203-S8A-T	(176 U3	ARLIN		Inv	1
3	>200-0406-100	SOCKET 40 P .6 ICO-406-S8A-T	(60 U1,U4	ARLIN		Inv	2
3	>201-0036-010	HDR 1X36 UN TSW-136-07-G-S	J3,J4=1X2	ARLIN		Inv	.111
3	>201-0050-021	HDR 2X25 ST PRO IDH-50LP-S3-TG/T	J2	ARLIN		Inv	1
3	>201-0050-121	HEADER RA 2X25 IDH-50LP-SR3-TG/T	J1	ARLIN		Inv	1
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J5=2X5	ARLIN		Inv	.138
3	>745-0245-200	IC, 74HCT245	U2	ARLIN		Inv	1
3	>400-0170-000	PCB, PCM-I/O 48 REV A	PCB, PCM-I/O 48 REV A	ARLIN		Inv	1
2	0170-300-0000	SUB ASSY PCM-1048 REV A	SUB ASSY PCM-1048 REV A	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	01-25-93 RC RELEASED	ARLIN		Inv	1
3	>801-0031-200	IC, 71055C PROG PAR INTERFACE	U1,U4	ARLIN		Inv	2
3	>901-0002-000	IC, EP320 PI	U3 CS=686C	ARLIN		Inv	1
3	>500-0200-001	SCREW 2-56 X 1/4 PPH	SCREW 2-56 X 1/4 PPH	ARLIN		Inv	2
3	>500-0200-091	SPACER M/F RAF 4000-440-N-MODL.6	SPACER M/F RAF 4000-440-N-MODL.600	ARLIN		Inv	2
3	>500-0200-092	NUT HEX NYLON 4-40	NUT HEX NYLON 4-40	ARLIN		Inv	2
2	950-0002-000	BAG PINK POLY 6X10 SC9061	BAG PINK POLY 6X10 SC9061	ARLIN		Inv	1

REPORT RECAP

0 WARNING(S) * Indicates no BOM Found for Item
0 ERROR(S)

REPORT PARAMETERS

ASSEMBLY RANGE : PCM-1048 to PCM-1048
TYPE : <ALL>

DESC LENGTH: ITEM : 32
COMMENT : 40
LOCATION: 0
OVERHEAD: 0

COMPONENT RANGE : <FIRST> to <LAST>
TYPE : RWF

NESTING INDENT LENGTH: 20

MASKING : Inv-Explode Specific Inv Items (No Masks)

TOTAL REPORT WIDTH : 132

QUANTITY (TO EXPLODE): 1