T3-3002
Safety Board CPLD Programming Guide
Revision: -
TABLE OF CONTENTS

1 PROGRAMMING GUIDE OVERVIEW.................................................................................. 3
2 EQUIPMENT AND TOOLS REQUIRED............................................................................ 3
3 EXPLANATION OF XILINX PROJECT FILES................................................................. 3
4 TEST SETUP................................................................................................................... 3
5 PROGRAMMING ............................................................................................................. 4
   5.1 START XILINX ISE & OPEN PROJECT ....................................................................... 4
   5.2 IMPLEMENT DESIGN .................................................................................................. 5
   5.3 PROGRAMMING THE CPLD ...................................................................................... 6
6 COMPLETION.................................................................................................................. 11

TABLE OF FIGURES & REPORT TABLES

FIGURE 1 HARDWARE PROGRAMMING SETUP.................................................................. 4
FIGURE 2 XILINX ISE MAIN WINDOW............................................................................... 4
FIGURE 3 XILINX ISE WITH PROJECT OPEN.................................................................... 5
FIGURE 4 EXPANDED “PROCESSES” WINDOW................................................................ 5
FIGURE 5 “IMPLEMENT TOP MODULE” COMMAND......................................................... 6
FIGURE 7 IMPLEMENTATION COMPLETION SCREEN....................................................... 6
FIGURE 8 PROGRAMMING IMPACT WINDOW................................................................... 7
FIGURE 9 ASSIGN CONFIGURATION FILE......................................................................... 7
FIGURE 10 MAIN PROGRAMMING WINDOW................................................................. 8
FIGURE 11 PROCESS SELECTION WINDOW..................................................................... 9
FIGURE 12 ERASE OPTIONS WINDOW.......................................................................... 9
FIGURE 13 ERASE PROGRESS WINDOW....................................................................... 10
FIGURE 14 PROGRAMMING PROPERTIES WINDOW....................................................... 10
FIGURE 15 PROGRAMMING PROGRESS WINDOW......................................................... 11
FIGURE 16 TRANSCRIPT WINDOW.................................................................................. 11

TABLE 1 REQUIRED EQUIPMENT.................................................................................... 3
TABLE 2 REQUIRED XILINX FILES................................................................................ 3
1 Programming Guide Overview

This programming guide will give all the steps to program the Safety Board CPLD. If any modifications are required to the CPLD logic, the main schematic used for this project may be modified and saved. Then, follow all steps outlined below.

Note: a simpler, programming only solution could have been employed, but since this is low, non-production type of programming, going through all the steps from the start using the schematic seems to be a more flexible approach that allows CPLD logic modification.

Also, the screen shots shown below may not match exactly depending on the version of the ISE software used, however, at the time of this document versions 9 and 10 were very similar in look an operation.

2 Equipment and Tools Required

The table below lists the equipment and tools required to complete programming.

<table>
<thead>
<tr>
<th>Item #</th>
<th>Qty</th>
<th>Model / Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Xilinx ISE Software 10.1</td>
<td>Xilinx Software for Design &amp; Programming</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>Xilinx DLC9 Platform Cable USB</td>
<td>TCS3 Lab System</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>+5V TCS3 Power Supply</td>
<td>+5V Power for Safety Board</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>Safety Board</td>
<td>Safety Board to be programmed</td>
</tr>
</tbody>
</table>

Table 1 Required equipment

3 Explanation of Xilinx Project Files

Before continuing to the setup section, the required Xilinx ISE project files should be explained. There are many files that are created automatically when using Xilinx ISE and this can be confusing when first using the tool. Below are the required files for the project. Any other files present in the directory may be deleted if desired or can be ignored. All files are contained in the main directory, “Safety_Board_Rev_C”, for example. All other subdirectories may be deleted or ignored. Rev C is used in the examples. If a higher revision exists, substitute that revision for Rev C.

<table>
<thead>
<tr>
<th>File</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Safety_board_rev_c.ise</td>
<td>Main Xilinx ISE project file.</td>
</tr>
<tr>
<td>Safety_brd_CPLD_schematic.sch</td>
<td>ISE Safety Board CPLD Logic Schematic file</td>
</tr>
<tr>
<td>logic_locked.ucf</td>
<td>CPLD pinout assignment &amp; timing constraints</td>
</tr>
<tr>
<td>Rev_Block_Main.sym</td>
<td>Symbol for main rev block used in schematic.</td>
</tr>
<tr>
<td>Rev_Block.sym</td>
<td>Symbol for rev block used in schematic.</td>
</tr>
<tr>
<td>IFA_Title_Block.sym</td>
<td>Symbol for title block used in schematic.</td>
</tr>
<tr>
<td>cpld_all_scm.pdf</td>
<td>NOT REQUIRED Useful PDF of all design elements in Xilinx library for CPLD.</td>
</tr>
</tbody>
</table>

Table 2 Required Xilinx files.

4 Test Setup

Follow these steps to setup for programming:

1. Install Xilinx ISE Software if not already installed.
2. Connect the Xilinx Platform Cable USB DLC9 to the PC via USB and to the Safety Board JTAG header via the ribbon cable (red dotted wire on ribbon represents pin #1).

3. Connect the +5V power supply to the Safety Board. Apply power.

5 Programming

5.1 Start Xilinx ISE & Open Project

1. Start the Xilinx ISE software.

5.2 Implement Design

1. Expand the “Implement Design” heading in the “Processes” window. Then expand the sub-heading “Generate Programming File”.

Figure 3  Xilinx ISE with project open.

Figure 4 Expanded “Processes” window.
From the Processes menu, select (right click) Implement Design->Rerun All.

![Screen shot of Processes menu]

Figure 5 “Rerun All” command.

The blue arrows in the “Processes” window under “Implement Design” will begin to rotate. When the ISE tool is finished with the final step of generating the program file, the window will look like:

![Implementation completion screen]

Figure 6 Implementation completion screen.

5.3 Programming the CPLD

1. Select (double click) on “Configure Device (IMPACT)” in the “Processes” window. Select “Configure devices using Boundary-Scan (JTAG)”. Click Finish.
2. A window will automatically pop up. Select “Safety_brd_CPLD_schematic.jed”. This file was automatically created by ISE. Click Open.
The window will now look like:

Figure 9   Main programming window.
3. Select “Program” via a right mouse click on the green graphic of the CPLD or under the “Processes” window.

![Process selection window](image)

Figure 10  Process selection window.

4. Erase CPLD (optional). If the CPLD is new, it may not have write protection on. However, if this is a part that was previously programmed for the Safety Board, it will likely have write protect on. This requires a separate erase cycle. Select “Erase” via a right mouse click on the green graphic of the CPLD or under the “Processes” window.

![Erase Options window](image)

Figure 11  Erase Options window.
5. Select “Program” via a right mouse click on the green graphic of the CPLD or under the “Processes” window. From the window that pops up, select “Verify”, “Erase Before Programming”, and “Write Protect”.

Note: “Write Protect” is used because as Xilinx states, “The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up.”

Figure 12 Erase progress window.

Figure 13 Programming Properties window.
A progress window will pop up.

![Progress Dialog](image)

Figure 14  Programming progress window.

Upon completion, the “Transcript” window should have an indication that says “Programming completed successfully”.

![Transcript Window](image)

Figure 15  Transcript window.

6 Completion

The CPLD is now programmed. Power down the +5V supply and disconnect the programmer. The Safety Board must now be tested using the Safety Board Test Procedure before it is to be used in the IRTF TCS.