Adapting ARC (Leach) Controllers for Use with HAWAII and Aladdin Arrays

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Overview

- Main goal is to cover physical modifications made by IRTF to ARC controllers
- Intended to be a practical “How To” guide to implement the ARC controller
- Modification rationale explained
- Performance results
Controller Background

- ARC controllers are general purpose array controllers sold by Astronomical Research Cameras Inc.
  - Two sizes - 6 or 12 slot
  - Controllers configured for array type and channels
- Many observatories use ARC controllers
- IRTF uses for H2RG and Aladdin arrays
- Don Hall is presently evaluating for H4RG
ARC 32 CH H2RG Controller Setup

- Video Board 3 (CH 24-31)
- Video Board 2 (CH 16-23)
- Video Board 1 (CH 8-15)
- Video Board 0 (CH 0-7)
- Bias Board (IRT F made)
- Clock Driver Board
- Fiber Optic Timing Board

Video Boards AGND normally connected to this point.
(disconnected in picture)
ARC 8 CH Aladdin Controller Setup

Video Board 0 (CH 0-7)
Clocking Board
Bias Board (IRTF made)
Fiber Optic Timing Board

Still testing, but most likely Bias Board won’t be required and all biases will come from Clocking Board.
## IRTF Modifications Table

<table>
<thead>
<tr>
<th>#</th>
<th>Modification</th>
<th>H2RG</th>
<th>Aladdin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Custom Analog Bias Board</td>
<td>X</td>
<td>*</td>
</tr>
<tr>
<td>2</td>
<td>Video Card Ground Wires to Chassis</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>Output Source Follower RC</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>Video Board Gain Resistor Change</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>+36V Power Control Board Check Disabled</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6</td>
<td>Bulk Capacitor on -16.5V (startup current trip)</td>
<td>X</td>
<td>**</td>
</tr>
<tr>
<td>7</td>
<td>Used Agilent N6700B Power Supplies</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

* Noise performance of Aladdin << H2RG, should not be required
** Aladdin uses one Video Board, startup current is much lower, not required
Mod #1: Custom Analog Bias Board

● This is the most important modification
● This solves two issues
  ○ Long term drift (minutes) from Video Board biases
  ○ Low frequency noise (<100 Hz)
● Australian National University provided their complete design as a basis to start from
  ○ Huge help - provided CPLD logic to control board
Mod #1: Bias Drift Reduction

- Bias drifts affect array output over long integration periods (minutes)
  - Bias drifts result in output signal drift (noise)
  - Non-destructive reads (NDRs) not as effective
- The bias board reduces drift by using
  - Low drift reference (ADR4533BRZ - 2ppm/°C max)
  - Low drift DAC (AD7568BSZ - 5 ppm FSR/°C max)
  - Low drift op-amp (OP484FSZ - 2 μV/°C offset max)
  - Separate board = lower power and temperature
Mod #1: Low Frequency Bias Filter

- Low frequency noise present during darks
  - Appeared as banding across readout (<100 Hz)
  - Low level, but significant when dark
- Used low frequency RC filter on biases
  - VBIASPOWER and VBIASGATE most important
  - VBIASPOWER current draw is 100s of uA
    - Large R causes voltage drop due to current
  - VBIASGATE is nearly zero (gate of FET)
Mod #1: Bias Filter RCs

10 Ω resistor used on other channels for commonality since impact was minor. Only VBIASGATE requires low value resistor. If too large, there is a long ramp at beginning of readout due to channel output drawing a different current and the long time constant to reach steady state.

*VBIASGATE is almost zero current. It shouldn’t require a large capacitor. Why then?

We installed a capacitor between VBIASPOWER and VBIASGATE on the Cryogenic Configuration Board. This was found to be a mistake and required heavy filtering on VBIASGATE to compensate for this. Since an external solution was found, we decided not to open up NSFCAM to remove it.

2200 uF Tantalum  100 uF Ceramics  10 Ω resistor

VBIASPOWER  VBIASGATE  DSUB  VRESET  VDDA

fc=6 Hz for 2600uF  fc=40 Hz for 400uF
Mod #2: Video Card Ground Wires

- Suggested by Shane Jacobson
- Reduced noise by ~2-3 ADU for dark reads
  - Didn’t explore reason in detail
  - There is ground star point on power board so it shouldn’t be necessary, but mod works well
Mod #3: Output Source Follower RC

- Provides current for output source follower
- Bias derived from Video Board
  - Simpler cabling if Bias Board not used for this bias
  - Array not extremely sensitive to this bias normally
- When bright objects saturated an array channel on NSFCAM, “ghosting” occurred on other channels on same Video Board due to shift in bias voltage
There was a significant divider with 1k and 1.25k (10k/8). Current draw on channels significantly affect voltage which causes ghosting. Bias voltage is recommended to be +3.3V. Choose lower resistance value such that it forms an insignificant divider. Increase capacitor to still provide some filtering.
Mod #4: Video Board Gain Resistor

- Tailored integration gain resistor for “low gain” setting (bright objects)
  - Used 1.37 kΩ
  - Maximized dynamic range
- Default 1 kΩ for high gain
Mod #5: +36V Power Check Disabled

- +36V supply is not used by H2RG or Aladdin
- Disabled +36V check
- Cut pins U5-1&2
Mod #6: Bulk Capacitor on -16.5V

- ARC controllers have no “soft start” circuitry
- Startup current high with 5 Video Boards
  - Due to charging capacitors
  - Causes overcurrent trip
- Install 6800uF(25V) cap
- Could use larger supplies
  - Cost more
  - Not necessary
Mod #7: Agilent N6700B Supplies

- High quality supplies with ethernet

<table>
<thead>
<tr>
<th>Modules</th>
<th>Power Supplied</th>
</tr>
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<tbody>
<tr>
<td>N6743B (100W)</td>
<td>+16.5V</td>
</tr>
<tr>
<td>N6732B (50W)</td>
<td>+5V Digital, +6.5V, -6.5V</td>
</tr>
<tr>
<td>N6733B (50W)</td>
<td>-16.5V, 12V Fan</td>
</tr>
</tbody>
</table>
H2RG Wiring

Channels setup differentially. CH- is ground at Cryo PCB.

Cryo Config board keeps digital and analog grounds separate.

Analog biases (5 total) filtered on PCB with 100uF and 0.1uF ceramic. No resistor.

VDD (derived from clock board) also has 100uF and 0.1uF capacitors. No resistor.

Copper ribbon wires used for GNDs. (for channel ribbons = windowout & ref)
H2RG Wiring Hardware

Inside Mount
H2RG Clocking

- Clocking is fairly “standard”
- Normal pixel readout rate 200 kHz
  - Support for 100, 200, 300 kHz
H2RG Noise Results

- Used science grade H2RG (degraded slightly by Indium migration)
- Results obtained by selecting 40 pixel by 40 pixel area in array that was free of defective pixels
- Standard readout noise is essentially the pixel readout noise
- Slow readout using NDRs is dominated by pattern noise since it is the change in value of a pixel over a long series of readouts

<table>
<thead>
<tr>
<th>Readout Mode</th>
<th>Noise Requirement</th>
<th>Measured</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cryostat Standard</td>
<td>&lt;=15e-</td>
<td>11e-</td>
<td>COAD=1, NDR=1</td>
</tr>
<tr>
<td>NSFCAM Standard</td>
<td>&lt;=15e-</td>
<td>15e-</td>
<td>COAD=1, NDR=1</td>
</tr>
<tr>
<td>Cryostat Slow (30s)</td>
<td>&lt;=5e-</td>
<td>3.1e-</td>
<td>COAD=1, NDR=16, 30s</td>
</tr>
<tr>
<td>NSFCAM Slow (30s)</td>
<td>&lt;=5e-</td>
<td>4.4e-</td>
<td>COAD=1, NDR=16, 30s</td>
</tr>
</tbody>
</table>
Aladdin Noise Results

- Cold Aladdin readout using PAIDAI October 2013
- Results look good
- Need to verify device properties to ensure that our noise numbers are accurate before presenting
ARC H4RG Evaluation

- Don Hall is evaluating the ARC controller for the H4RG (4k x 4k) with 64 Channels
- Currently in warm mux bench test phase
- 64 channel readout successful October 2013
- Cooling down a mux in November 2013
ARC 64 CH H2RG Setup

Frontplane seemed like best solution vs. wired cabling with NANO connectors.

Supports:
- 32 or 64 CH readout
- Up to 9 Video Boards
- IRTF/ANU Bias Board

Due to 8 Video Boards, stock ARC power supply is undersized. More power required.
WARM H4RG 64 Channel Readout